Wideband Doherty Power Amplifier Design and Implementation

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***Abstract*—Key design considerations and measurement results for a 500-900 MHz Doherty power amplifier (DPA) are discussed in this report. Broadband matching/stabilization techniques are employed throughout the design procedure. A wideband output combiner with maximally flat response is designed to achieve the desired load modulation over targeted bandwidth (BW) while considering knee voltage effect for maximum back-off efficiency. The proposed design was implemented using packaged 10W Cree Gallium Nitride transistors. The designed DPA exhibited 6dB back-off efficiency higher than 45% and peak drain efficiency higher than 63% while delivering an output power of 43 dBm. The PA demonstrates more than 40% drain efficiency over an output back-off range of 8dBm over the entire BW.**

***Index Terms* — Bandwidth, broadband operation, Doherty combiner, Doherty power amplifier, efficiency, wideband.**

I. Introduction

Continuously evolving communication systems have led to development of new standards that pose significant challenges to power amplifiers (PAs). Base stations impose linearity requirements while modern communication standards with high peak-to-average power ratios (PAPRs) force PAs to operate at large back-off levels. Such conditions greatly degrade PA efficiency [1]. Among the many efficiency enhancement techniques, Doherty PAs deliver power efficient performance and are widely used for commercial purposes because of their ease of implementation.

The basic operation principle of DPA is well described in [2]. Fig. 1 shows the block diagram of a two-way symmetrical Doherty system. It comprises of an input power splitter, two amplifying cells (carrier and peaking) and an output combiner. Doherty architecture delivers high efficiency by turning off the peaking cell for low input power operation. The input power level corresponding to turn on of peaking cell is the Doherty transition point. Beyond this drive level, the peaking cell increasingly contributes to output power while the carrier amplifier remains saturated. Turn on of peaking cell initiates active load modulation such that both cells operate into optimum load value (R_{opt}) at peak input power level. By virtue of this mechanism, high efficiency is maintained over output power range from $P_{sat,dBm} + 20\log_{10}(\alpha)$ to $P_{sat,dBm}$, where α ($0 < \alpha < 1$) defines the Doherty transition point.

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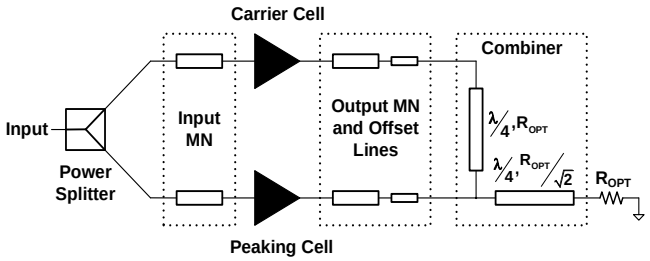

Fig. 1. Block diagram of a conventional 2-way symmetric DPA (MN - Matching Network).

In addition to high PAPR values, next generation signals occupy broader bandwidths (BWs). Doherty architectures have disadvantages in broadband application due to frequency dependent circuit components. The quarter-wave lines in output combiner can be optimized for only a narrow BW to achieve the correct load modulation for back-off performance. A phase-offset line at the input is also required to align the delay between the carrier and peaking paths. Stability/matching networks also impose limitation on operational BW.

Thus, designing and implementing a broadband DPA remains a challenge and has garnered much research attention. This report summarizes the key design considerations and results for a 500 – 900MHz broadband Doherty PA.

II. Design

The performance of the carrier cell, peaking cell and the output combiner are analyzed individually to address the challenges of broadband implementation. All simulations have been carried out in Advanced Design System 2013 software package. 10W GaN HEMT CGH40010F transistors are used for carrier and peaking cells.

A. Carrier Cell Design

Since the overall performance of the DPA is largely dominated by the carrier amplifier, a careful in-depth analysis is imperative. A broadband input matching network is designed using S-parameter simulation to prevent oscillations and ensure wideband matching. The amplifier is biased in class-AB with drain to source bias voltage, V_{DS} = 28V and quiescent current, I_{DQ} = 200mA. Optimum load impedance (R_{opt}) is determined through load pull measurements to realize a good trade-off between linearity, output power and efficiency.

B. *Peaking Cell Design*

The carrier cell matching network is re-used since the same CGH40010 device is used in both cells. Biasing is adjusted (class-C bias) according to the desired Doherty transition point such that the peaking cell remains off for low input drive levels.

An important design consideration that must addressed in DPA design is the problem of power leakage at large output back-off levels. To alleviate this issue, the dc-feed inductor of the drain bias line is tuned to present large output impedance at peaking cell.

C. *Output Combiner Design*

To maintain high efficiency over 6dB OPBO range (Doherty transition point, α = 0.5), the carrier cell must be presented with a load of $2R_{opt}$ prior to peaking transistor's turn-on. However, based on the knee voltage profile of the transistor, a load slightly more than $2R_{opt}$ is required to saturate the carrier cell at 6 dB back-off [3].

A wideband combiner with maximally flat frequency response based on [4] is designed to achieve the desired active load modulation. To match the output load R_{opt} to a 50 Ω termination, a 2-section Chebyshev network is used.

III. Results and Conclusions

The DPA design discussed in this report was fabricated as shown in Fig. 2. To evaluate the performance of the DPA, drain efficiency, output power and gain were measured under continuous wave signals. Fig. 3 and 4 report the measured performance of the fabricated DPA.

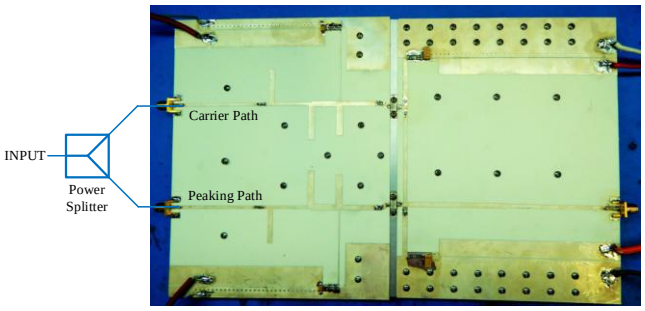

Fig. 2. Fabricated Doherty PA circuit.

The measured data confirms that the designed DPA achieves good performance over targeted frequency range. The DPA delivers a total output saturation power of approximately 43 dBm with a small signal gain of 14.2 dB. Drain efficiency above 45% and 63% is achieved at the 6dB OPBO and at peak power, respectively. The PA demonstrates higher than 40% efficiency over an OPBO range of 8 dBm for the entire bandwidth.

The results obtained in this research work demonstrate how the Doherty architecture can be adapted to achieve a good solution for broadband microwave power amplification, thereby making it a suitable candidate for base station applications.

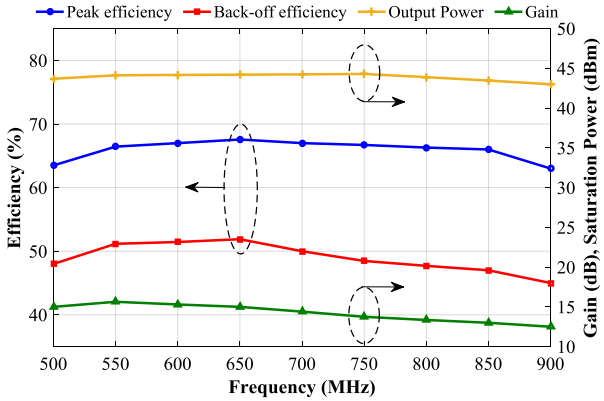

Fig. 3. Measured peak efficiency, 6-dB OPBO efficiency, output saturation power and small signal gain.

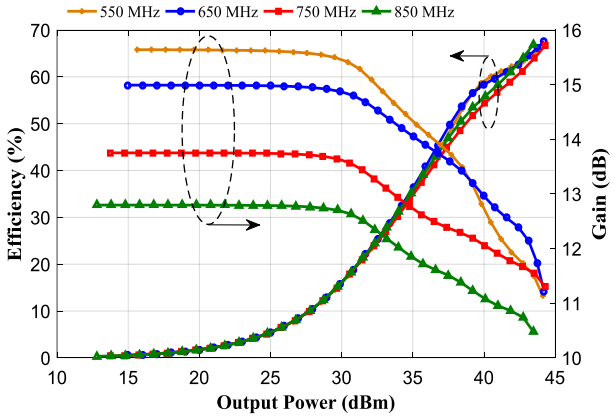

Fig. 4. Measured drain efficiency and gain profile versus output power.

IV. Impact Statement and Career Plans

I would like to acknowledge the IEEE MTT-Society for funding this research. Through this scholarship, I also had the opportunity to attend IMS2016 where I interacted with leading professionals and learned about exciting research. Such immense motivation enabled me to extend this research beyond the initial outlined objectives which has resulted in a journal paper (currently under review).

I am currently an Analog Design Engineering Intern at Semtech Corporation and will be resuming 4th year of undergraduate studies in Sept. 2017. I plan to pursue a graduate degree in high speed IC design. Having experience in PA as well as IC design, I am also interested in developing System-on-Chip solutions for RF power amplifiers.

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