

# Low Power V-Band Beamforming Transceivers for High Data Rate WiGig Applications

Pawan Agarwal, *Student Member, IEEE*, Deukhyoun Heo, *Member, IEEE*

**Abstract**—A brief project update and resulting outcomes are presented, for the research proposed under the IEEE MTT-S graduate fellowship award 2014-15. In this work, we proposed to investigate highly energy-efficient V-band beamforming transceiver architectures for high data-rate WiGig applications. We demonstrated a four-channel V-band, LO phase-shifting based sub-harmonic injection locked beamforming receiver with almost an order of magnitude reduction in power consumption. The next step is building high performance, ultra-low power signal generation using digitally-controlled oscillators (DCOs) and all-digital phase-locked loops (ADPLLs). A wide-tuning range, low power oscillator prototype was designed and will be integrated within ADPLL. Current research focus is on the design of beamforming transmitter. This work has, so far, resulted in 5 conference papers, including a nomination for the best student paper award at IMS 2015, Phoenix.

**Index Terms**—Beamforming transceivers, Sub-harmonic injection locked oscillators, Low-noise amplifiers, SPDT switch, Phase-locked loops.

## I. INTRODUCTION

The unlicensed 8-10 GHz bandwidth available in V-band all over the world has led to the possibility of designing commercial multi-gigabits wireless communication applications [1]-[3]. Such high data rate communication can open the door for new applications like instant wireless sync between devices, wireless LAN etc. However, for wide adoption in mobile devices, power consumption of such systems needs to be reduced by at least an order of magnitude. Additionally such low power system can be easily re-optimized to operate at other mm-wave bands (e.g. E-band).

The design of millimeter wave wireless circuits in silicon for any sensible distance coverage poses its own challenges. Beamforming has emerged as the most feasible approach due to the increased antenna gain and reduced interference. Beamforming can be achieved by the use of either digital phase shifting, RF phase shifting or LO phase shifting. Digital beamforming is a powerful technique for multiple beam systems, but it suffers from the low input dynamic range. RF phase shifting alleviates the problem of LO distribution over multiple channels, but requires RF phase shifters that have high losses in the signal path. Since phase shifting loss needs to be compensated to achieve higher dynamic range and low noise figure, additional gain stages are required which can

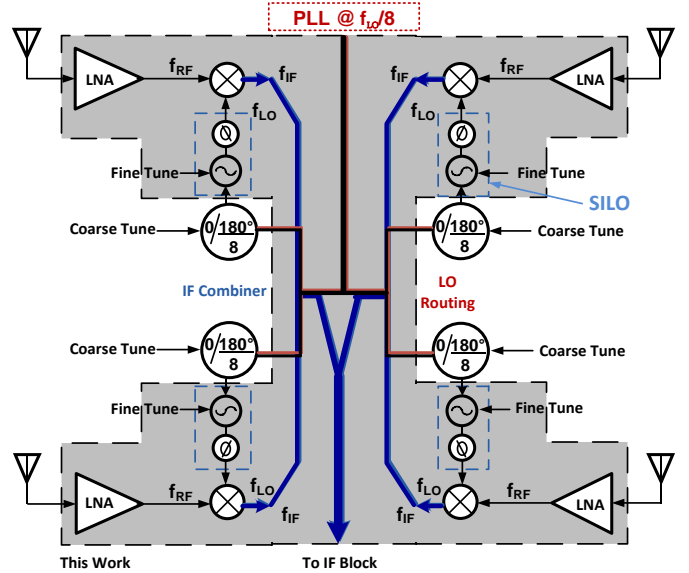


Fig. 1. Block diagram of the proposed 4-channel beamforming receiver using LO phase-shifting [4].

significantly increase the power consumption. Traditional LO phase shifting approaches are limited by the dynamic range of mixers as well as LO distribution, which results in higher power consumption.

Hence, the objective of this research is to investigate the design of low power mm-wave beamforming architecture using LO phase-shifting. A sub-harmonic injection locked oscillator with phase-shifting capabilities was proposed in [3]-[4] for beamforming systems. A novel feed-forward transformer coupled LNA was proposed to minimize the noise figure of the receiver without additional power penalty [5]. The proposed receiver consumes a minimum power of only 11.4 mW with minimum NF of 7.7 dB. In addition, a 25 GHz voltage controlled oscillator with 34.8% tuning range with only 4.1 mW power consumption was designed to generate the sub-harmonic LO signal using switched-substrate shield inductor [6]. Using the proposed architecture with novel ultra-low power sub-blocks, overall system power consumption can be significantly reduced while improving the performance.

## II. PROJECT OUTCOME

The block diagram of the proposed beamforming transceiver is shown in Fig. 1. Significant power and area savings can be achieved by sharing the LO distribution network across all the channels. Driving mm-wave LO signal

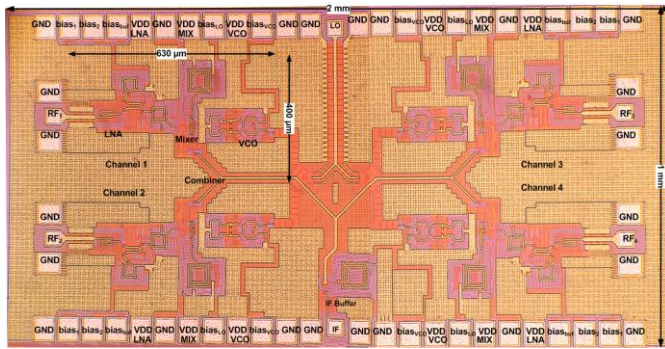


Fig. 2. Micrograph of the four-channel beamforming receiver. Total area is 1 X 2 mm<sup>2</sup> [4].

through such a large routing network can result in significant loss. Traditionally, LO buffer's power consumption is scaled to mitigate these losses. We proposed to use a LO distribution network operating at sub-harmonic LO frequency, thus reducing the routing loss [3]-[4]. By using the integrated frequency-multiplier and phase-shifter, the mm-wave LO signal is generated within each channel for up/down conversion by the mixer. To further minimize frontend power consumption, a feed-forward transformer coupled LNA was proposed [5].

The proposed topology utilizes an 8<sup>th</sup> sub-harmonic LO routing scheme. The micrograph of the 4-channel receiver prototype is shown in Fig. 2. The receiver consumes a minimum power of only 11.4 mW in each channel while providing a peak gain of 8.3 dB with minimum NF of 7.7 dB. Peak beamforming gain of the receiver, measured using 2 channels simultaneously, is 5.4 dB (in-phase) and a minimum gain of -12.5 dB (out-of-phase). As the need for sLO and LO buffer is eliminated, an order of magnitude reduction in power consumption is achieved compared to the state-of-the-art designs.

Additionally, a wide tuning range CMOS VCO based on a switched substrate-shield inductor was proposed. Due to the minimized substrate losses and parasitic capacitances, the VCO has a higher loaded tank quality factor and larger varactor based tuning range. Using the proposed design, a 29 % inductance switching is achieved while maintaining a high quality factor of > 15.5. The VCO's chip micrograph shown in Fig. 3. The prototype shows an excellent frequency tuning range of 34.8 % and a phase noise of -120.1 dBc/Hz at 10 MHz offset for 25.3 GHz carrier frequency. This VCO has a FOM<sub>T</sub> of 192.1±2.5 dBc/Hz across the tuning range with only 4.1 mW power consumption. The VCO shows lowest power consumption and highest figure-of-merits among state-of-the-art designs for mm-wave applications. Owing to its low power and scalable nature, the proposed beamforming architecture is most suited for next generation low power high data-rate mm-wave wireless communication applications.

### III. CAREER PLANS

First, I would like to sincerely thank IEEE Microwave Theory and Techniques Society (MTT-S) for granting me the honor of the prestigious MTT-S Graduate Fellowship Award.

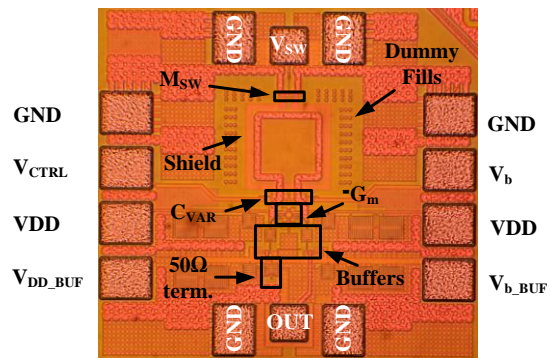


Fig. 3. Chip Micrograph of the switched substrate-shield inductor based VCO [6].

This fellowship has provided me the opportunity to closely examine some of the toughest problems in the area of high-speed wireless communication. Upon graduation, I hope to utilize this experience to continue exploring these problems in an industrial teamwork environment, where the solutions can be readily delivered to the end user for an improved life experience.

### IV. IMS IMPRESSION

IEEE International Microwave Symposium (IMS) 2014 provided me the opportunity to not only present my research work [5] [7], but also proved to be a great venue for deeply technical discussions with some of the best minds in the field of microwave engineering. I am looking forward to IMS 2015, Phoenix, to present my current research work [6] and continue the tradition of insightful discussions to improve my work.

### V. REFERENCES

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