Digital Phase Shifter With High Phase Accuracy for Microwave Phased Array Application

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***Abstract*—Surrounding the application requirement of microwave communication system with merits of lower power consumption and higher data rates, this project investigates digital phase shifter with high phase accuracy for smart microwave phased array application. In this project, an 8-bit digital phase shifter using vector-sum architecture is presented. A common-gate common-source (CG-CS) active balun and a 2-stage poly-phase filter (PPF) are utilized for differential and quadrature signals generation, respectively. Meanwhile, four identical VGAs using digital control DAC cell are combined for amplitude modulation and vector summation. To verify the mechanism mentioned above, the proposed digital phase shifter is simulated based on a 28nm CMOS technology, which features a maximum RMS phase error of 0.66° and a maximum RMS gain error of 0.19 dB from 18 GHz to 24 GHz. Additionally, the proposed digital phase shifter exhibits a peak gain of 8.8 dB with 15 mW power consumption.**

***Index Terms*—Digital phase shifter, active balun, poly-phase filter, vector-sum, phased array.**

I. Introduction

With the ever-increasing application requirement of wireless communication system, microwave phased array system shown in Fig. 1 is widespread [1]. Meanwhile, phase shifters with higher phase accuracy and lower power consumption are in great demand for higher quality beam-forming capability. Due to the merits of flexible control and no power consumption, switch-type phase shifter [2] and reflection-type phase shifter [3] are well developed in recent years. However, they suffer from large insertion loss and big chip area. To achieve a phase shifting characteristic with power gain and small chip area, on-chip digital vector-sum phase shifters are introduced [4], [5]. Nevertheless, these phase shifters need an extra current control circuits for phase shifting control, which is not easy to be extended for higher phase resolution. Thus, this project introduces a novel VGA with digital control DAC cell to implement the digital phase shifter with the merits of power gain and high phase resolution. The proposed phase shifter shows an extremely low RMS phase error and gain variation in a small chip area, which is attractive for smart microwave phased array application.

II. Circuit Design

Fig. 2(a) presents the architecture of the proposed digital vector-sum phase shifter, which consists of five sections: an active balun, a 4-stage power driver, a 2-stage poly-phase filter (PPF), four identical VGAs with digital control DAC cell, and a differential to single (D2S) transformer. The radio-frequency signal is injected in the active balun and 4-stage power driver to obtain amplified differential signals with uniform amplitude. Then, the 2-stage PPF converts the differential signals to quadrature signals. Finally, quadrature signals are individually amplified and vector summed by VGA and D2S transformer to generate output signals with various phase shifting modulation.

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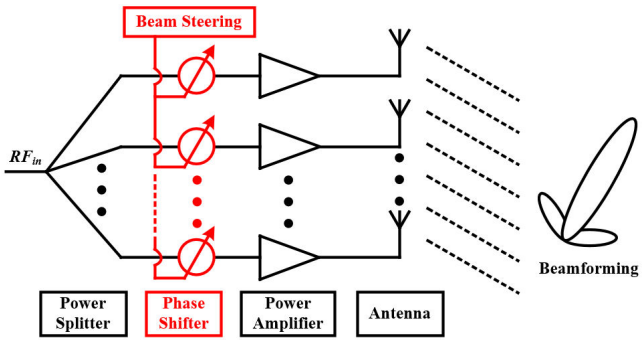

Fig. 1. Digital Phase shifter in a phased array transmitter system.

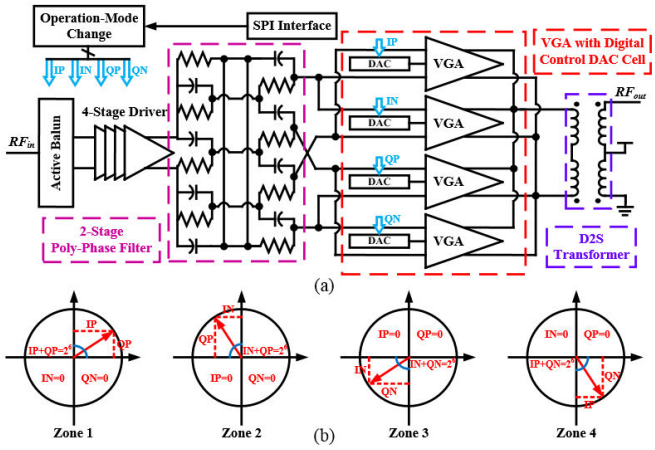

Fig. 2. (a) The architecture of the proposed vector-sum digital phase shifter. (b) Four zones of the phase shifter to cover 360° phase shifting.

A. Quadrature Signals Generation

Quadrature signals with low phase error and amplitude variation are critical for vector-sum phase shifter design. Meanwhile, in order to generate quadrature signals in a small chip area, the active balun using common-gate common-source (CG-CS) topology and 2-stage PPF based on R-C circuits are implemented. Four PMOS loaded common-source amplifiers are serial connected as a 4-stage power driver to compensate the loss introduced by the 2-stage PPF.

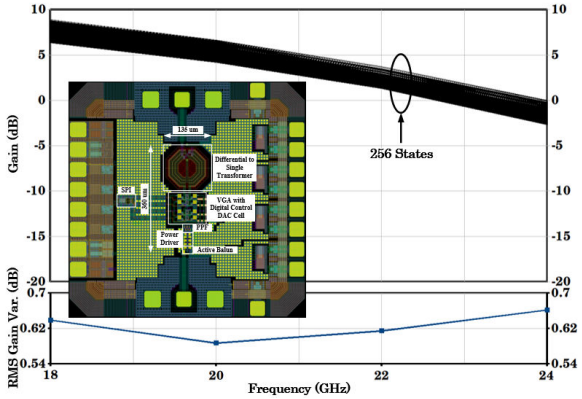

Fig. 3. Simulated gain results under 256 states, RMS gain variation, and layout of the proposed phase shifter.

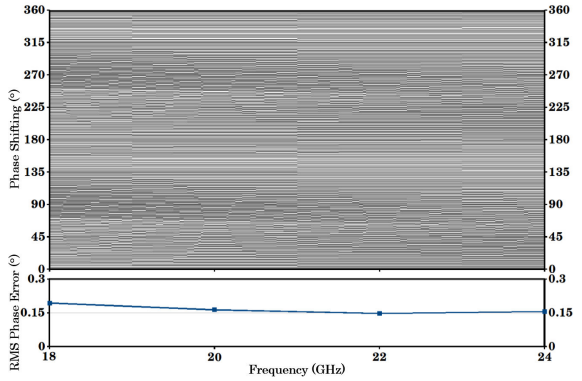

Fig. 4. Simulated phase shifting results under 256 states and RMS phase error of the proposed phase shifter.

B. VGA with Digital-Control DAC Cell

As for a vector-sum phase shifter, the phase resolution is mainly depended on the gain resolution of the VGA part. Consequently, for obtaining a high phase resolution, the VGA with digital control DAC cell is introduced. The gain generated by the VGA can be adjusted by turning on/off the MOSs with different ratio of width and length (i.e., W/L). The W/L of the MOSs are in geometric sequence, which means only six MOSs can achieve a 6-bit gain resolution. In order to implement a 360° phase shifting range, four identical VGAs with different differential signals injected are utilized. The 360° phase shifting range is divided into four zones. Only two VGAs work on and the rest are closed in one zones. The relationship between control code for DAC cell and four zones is depicted in Fig. 2(b). Then, an 8-bit phase resolution can be implemented by using these four 6-bit VGAs. Moreover, the phase resolution is easy to be extended just by increasing the quantity of MOSs in VGA.

III. Result

The proposed digital phase shifter was simulated in 28nm CMOS technology. The chip layout is shown in Fig. 3 and the core chip size is 0.36 mm × 0.135 mm. Fig. 3 and Fig. 4 depict the simulated S-parameter results for 256 phase states of the phase shifter. The peak gain is 8.8 dB. The minimum RMS gain variation is 0.59 dB at 20 GHz and <0.66 dB over 18–24 GHz. Meanwhile, The minimum RMS phase error is 0.15° at 22 GHz and <0.19° over the whole operational band. The overall power consumption in the digital phase shifter including SPI control circuits is 15 mW from a 1 V supply voltage. Table I summarizes and compares major performance with current state-of-the-art phase shifters.

TABLE I Performance Summary and Comparision

Ref.	**This work***	[2]	[3]	[4]	[5]
Frequency (GHz)	**18–24**	57–64	57–64	2-24	4.9–5.9
Technology	**28nm CMOS**	90nm CMOS	0.12um SiGe BiCMOS	65nm CMOS	0.13um CMOS
Resolution (bit)	**8**	5	6	7	6
Peak Gain (dB)	**8.8**	–10	–7.4	1	1
RMS Gain/Phase Error(dB/°)	**<0.66/<0.19**	<2/<10	<0.3/<2.6	<1.5/<1.22	<0.7/10
Power Consumption (mW)	**15**	0	0	92	28
Core size (mm^2)	**0.05**	0.34	0.28	1.18#	0.303

*Simulated results; #Estimated from the layout.

IV. Conclusion

In this project, an 8-bit digital phase shifter based on novel VGA using digital control DAC cell is proposed for smart microwave phased array application. Active balun and poly-phase filter are utilized for quadrature signals generation. Meanwhile, four identical VGAs and a differential to single transformer are employed for vector modulation and summation. Based on a 28nm CMOS process, The simulated results exhibit that the proposed phase shifter is featured with a maximum RMS phase error of 0.66° and a maximum RMS gain variation of 0.19 dB from 18 GHz to 24 GHz.

V. Acknowledgment and Next Plan

The IEEE MTT-S Undergraduate/Pregraduate Scholarship motivates and supports me to pursue research in the microwave [6], [7]. During the trip of IMS2018 in Philadephia, I got to know the speedy development of microwave in both academia and industry, which made me to fix my next plan to pursue a Ph.D. in the area of microwave integrated circuits.

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