Reconfigurable mm-Wave Watt-Level Digital Power Amplifier with Dynamic Load Modulation

K. Datta, *Student Member* and H. Hashemi, Senior *Member, IEEE*

***Abstract*— Reconfigurable power amplifier (PA) architectures to enhance transmitter efficiency under power back-off operation is investigated in this project. A tunable transmission line architecture has been proposed to implement a dynamic reconfigurable load modulation network that enables a digital PA to maintain high average efficiency while supporting modulations with high peak-to-average power ratios (PAPR). The proposed technique is demonstrated in a Watt-level mm-wave digital power amplifier fabricated in a 0.13 µm SiGe BiCMOS process. The designed IC shows a measured peak output power 29 dBm at 46 GHz with 18.5% peak PAE and a 11% PAE at 6 dB back-off. Preliminary ASK modulated measurements show dynamic operation at 500 MS/s.**

***Index Terms*— Power amplifier, SiGe, HBT, Class-E, transmission line, load modulation, amplitude shift keying, transmitter.**

I. Introduction

In recent years, there has been great interest in realizing mm-wave transceivers supporting multi-Gb/s wireless communication. To cover realistic link-lengths under high atmospheric attenuation at mm-waves, significant research has been conducted to generate Watt-level output power at mm-wave frequencies using silicon technologies. There also has been recent research into new transmitter architectures to support complex modulations for high data throughput while maintaining high peak efficiency by using highly efficient switching amplifiers at mm-waves. However since complex quadrature amplitude modulation (QAM) schemes like 64 QAM, 256 QAM etc., have high PAPR, a power amplifier architecture that can maintain high efficiency under deep power back-off is also critical to maintain overall average transmitter efficiency.

II. mm-Wave Digital Polar Transmitter

A digital polar transmitter is one of the proposed transmitter architectures [1] that utilizes the highly efficient switching power amplifiers like Class-E to function as unit cells to realize an overall linear transmitter. In this architecture (Fig. 1), the base-band information is split into amplitude and phase information for individual processing. The phase information is modulated using high-speed phase modulators at the mm-wave carrier frequency to be amplified and transmitted by the constant envelope Class-E power amplifiers. The amplitude information is used in the high-speed amplitude decoders that control how many of the Class-E PA unit cells would be power-combined to determine the overall output amplitude. This transmitter architecture thus recombines the amplitude and phase information at the output, supporting QAM modulation schemes while maintaining high peak efficiency by using highly efficient, nonlinear switching PA unit cells.

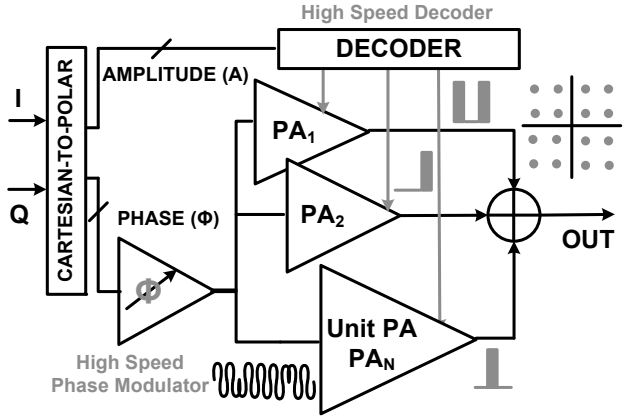

Fig. 1. A mm-wave digital polar transmitter architecture.

III. mm-Wave Class-E Power Amplifiers

Non-linear switching amplifiers like Class-E are more efficient than linear class of amplifiers like Class-A, AB due to their non-overlapping voltage and current waveforms. However at mm-waves, Class-E PA design becomes challenging as the proper amplitude and phase of the harmonics of the carrier frequency must also be maintained close to the f_T, f_{max} of the transistors. Several highly efficient mm-wave Class-E PA designs were demonstrated in [2] for use as unit power amplifier cells in a digital polar transmitter.

Apart from high collector efficiency, at mm-waves, a SiGe HBT Class-E power amplifier can generate higher power compared to linear class of amplifiers by supporting a higher transistor breakdown voltage. Since in a SiGe HBT, the transistor breakdown voltage is dependent upon collector

K. Datta, is with the Electrical Engineering Department, University of Southern California, Los Angeles, CA 90089 USA. (e-mail: kdatta@usc.edu).

H. Hashemi, is with the Electrical Engineering Department, University of Southern California, Los Angeles, CA 90089 USA. (e-mail: hosseinh@usc.edu).

current density, the non-overlapping Class-E waveforms enable the SiGe HBT collector voltage to swing upto BVCBO which is much higher than the nominal BVCEO [2]. Even higher power from a single unit PA was realized by stacking SiGe HBTs in a stacked Class-E design [2]. These moderate power highly efficient stacked Class-E PAs have been used to realize a Watt-level digital PA.

IV. Digital PA with Dynamic Load Modulation

In a digital polar transmitter, the amplitude decoder controls the number of unit PA cells to power-combine and determine the overall output amplitude. Thus for supporting modulation schemes like 64 QAM, 256 QAM etc., several of the individual unit PA cells must be turned OFF to cover the low amplitude constellation points. In this power back-off mode, the impedance seen by the remaining active unit PA cells is very different from the optimum impedance during peak power operation. This 'load-pulling' effect causes the efficiency of the remaining active unit PA cells to drop under power back-off resulting in severe degradation of transmitter efficiency under high PAPR conditions.

To mitigate the effect of load-pulling in a mm-wave digital power amplifier, a dynamic load modulation network is proposed that can maintain the optimum impedance presented to each active unit PA cell irrespective of the number of unit PA cells turned ON/OFF. A tunable transmission line architecture is proposed to achieve such reconfigurable power combining network. The tunable transmission line (Fig. 2) comprises of a signal line, a fixed ground plane and floating metal layer digitally controlled by MOSFET switches connected to the fixed ground plane. By toggling the MOS Logic 'High' or 'Low', the floating metal layer is either electrically shorted to ground potential or kept open. Thus the ground plane virtually moves UP or DOWN, varying the separation with the signal line and digitally controlling the characteristic impedance of the transmission line.

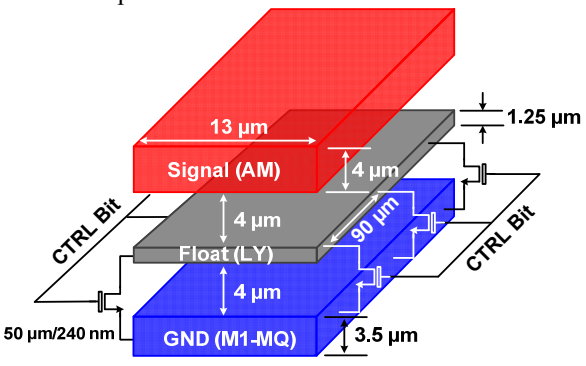

Fig. 2. A tunable transmission line with variable characteristic impedance.

The variable impedance transmission line is used to realize a 2:1 current combiner which is then 4-way current combined using a low loss, slow wave combiner (Fig. 3). As the different unit PA cells are turned OFF to achieve power back-off operation, the different tunable transmission line structures are put in 'High Z_C.' or 'Low Z_C.' impedance mode to enable each active unit PA cell to still see the optimum impedance ($Z_{OPT.}$) of the peak power mode and thus maintain the peak efficiency even under power back-off.

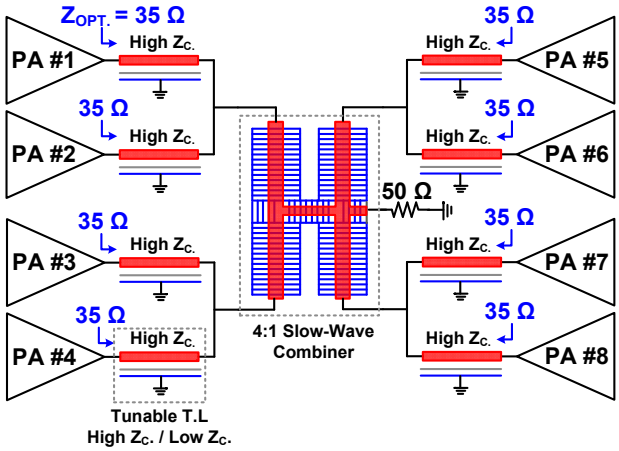

Fig. 3. Dynamic load modulation in 8-way combined mm-wave digital PA.

V. Implementation and Measurement Results

The Watt-level mm-wave digital PA with dynamic load modulation network [3] was designed and fabricated in 0.13 µm SiGe BiCMOS process (Fig. 4). The chip showed a measured peak output power of 28.9 dBm at 46 GHz with 18.4% peak PAE. Operation under power back-off, tested by toggling the 4-bit digital control codes demonstrated 11% efficiency at 6 dB power back-off (Fig. 4), highlighting the advantage of using the dynamic load modulation network.

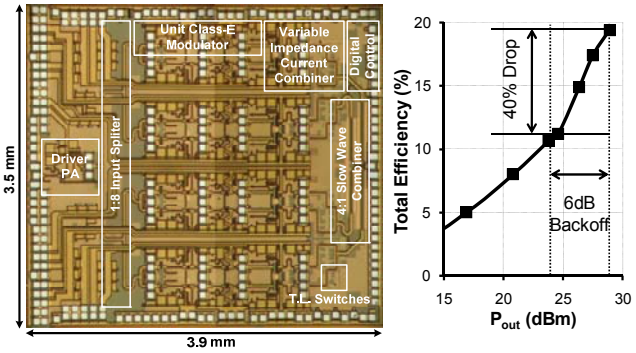

Fig. 4. Chip microphotograph and measured power back-off operation of the Watt-level mm-wave digital PA.

VI. Future Direction

My involvement in this project, enabled me to research new concepts and validate the results in a laboratory environment. I believe the skill sets I learned will be invaluable in both industry and academic settings. I am grateful to the IEEE MTT-S graduate fellowship award for making this project possible and enhancing the quality of my Ph.D. research.

References

[1] N. Singhal, *et. al*, "A digital envelope combiner for switching power amplifier linearization," in *IEEE TCAS-II*, April 2010.
[2] K. Datta, *et. al*, "Performance limits, design and implementation of SiGe HBT Class-E and stacked Class-E power amplifiers," in *IEEE JSSC*, Oct. 2014.
[3] K. Datta, *et. al*, "A 29 dBm, 18.5% peak PAE mm-wave digital power amplifier with dynamic load modulation," in *IEEE ISSCC*, Feb. 2015.