Mixed-Signal Hybrid Architectures for Efficiency and Linearity Improvement in Silicon-Based RF Power Amplifiers

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I. Introduction

Spectrum efficient modulations with high peak-to-average power ratios (PAPRs) and sophisticated power control schemes are widely employed in modern wireless systems. As a result, energy-efficient and linear operations up to the deep power back-off (PBO) region become essential for power amplifiers (PAs) to ensure the mobile device battery life and quality of service. Recently, mixed-signal PAs with *in-situ* digital computations implemented in scaled silicon processes have demonstrated their unique capability of enhancing the large-signal RF transmitter performance, including energy efficiency, linearity, and robustness against antenna impedance mismatch [1]-[5]. These digital-intensive architectures are also conducive to full system-on-chip (SoC) integration. However, employing individual PA efficiency enhancement technique often results in limited improvement at deep PBO levels, even when the digital-intensive PA architectures are utilized.

To address these challenges, we propose the concept of mixed-signal hybrid PA architectures that incorporate multiple efficiency enhancement techniques in a single PA to offer large PA efficiency enhancement over a substantially extended PBO range. PA linearity up to the deep PBO levels is ensured by mixed-signal operations. This concept was successfully demonstrated by a mixed-signal Class-G Doherty PA in our early research [6], [7]. However, the Doherty PA often requires substantial chip areas for the passive components. For example, two-inductor and one-inductor footprints are required for the Doherty output and input networks in [6], [7].

In this report, we describe our recent research progress on the mixed-signal hybrid PA partially supported by the 2015 IEEE MTT-S Graduate Fellowship. A mixed-signal PA with hybrid Class-G and dynamic load trajectory manipulation (DLTM) operations is presented [8]. A prototype implemented in a standard 65nm bulk CMOS process demonstrates superior efficiency and linearity up to the deep PBO region. Moreover, it only requires one-inductor area cost for all the passives.

II. Project Description and Research Outcome

Classic Class-G operation cannot support PA efficiency enhancement within each Class-G mode. Modulating the PA load impedance by a reconfigurable output network can enhance the PA PBO efficiency. However, conventional load modulation PAs face stringent design trade-offs among the complexity/area/loss of the passive network and the effective PBO range. Class-G and conventional load modulation operations may also lead to linearity issues by causing PA gain and phase discontinuities during the PBO. In our mixed-signal PA with hybrid operations of real-time Class-G and DLTM, PA efficiency is enhanced up to the deep PBO region without requiring a demanding impedance tuning range on the PA load modulation network. Moreover, a DLTM scheme is proposed to achieve PA efficiency peaking during the PBO. The PA linearity, including both amplitude and phase responses, is ensured by the mixed-signal PA operation.

Figure 1 shows the proposed mixed-signal hybrid Class-G and DLTM PA architecture. It comprises an RF power digital-to-analog converter (DAC), a Class-G supply modulator, and an on-chip load modulation passive network. The PA operates in a polar fashion. The RF power DAC is driven by the RF phase-modulated (PM) signal, and the amplitude modulation (AM) is synthesized by dynamically setting the power DAC, the Class-G modulator, and the load modulation network.

The hybrid real-time Class-G and DLTM operations for PA PBO efficiency enhancement are described as follows. At the peak PA output power (P_{out}) level, i.e., 0dB PBO, the supply is in the full-V_{DD} mode, and the PA load is set by the load modulation network to the optimum impedance generating the maximum P_{out} (Z_{opt_Pout}). Without changing the PA RF output

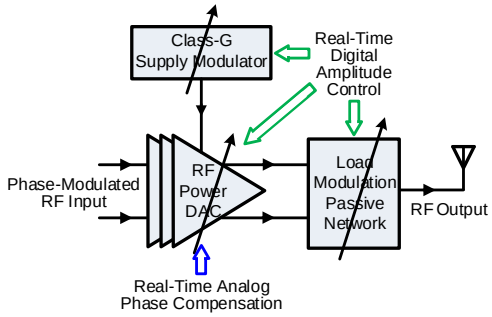

Fig. 1. Mixed-signal hybrid Class-G and DLTM PA architecture.

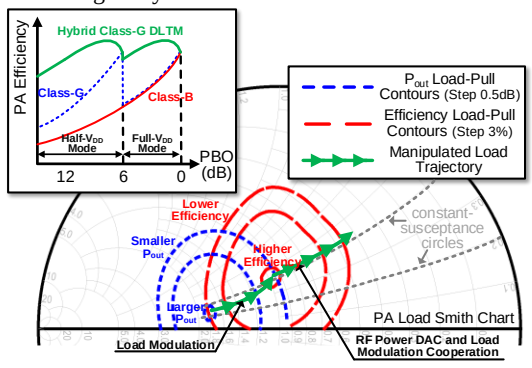

Fig. 2. PBO efficiency enhancement by hybrid Class-G and DLTM operations.

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current, i.e., the power DAC setting, the PA first performs its PBO operation by manipulating the load to travel from Z_{opt_Pout} to the optimum PA load impedance offering the maximum PA efficiency (Z_{opt_η}). During this process, the PA efficiency peaks and reaches the maximum value. For larger PBO levels, the power DAC then scales down the PA RF output current, and the load is simultaneously adjusted by DLTM with proper conductance along the constant-susceptance circle. The PA PBO efficiency is enhanced until the load tuning limit is reached. At 6dB PBO, the Class-G operation sets the supply to the half-V_{DD} mode. The above DLTM operation is then repeated for the PBO levels beyond 6dB. Note the digital-intensive PA architecture enables precise and optimum real-time hybrid PA operations that cannot be achieved by conventional analog PAs.

The PBO efficiency curve of the proposed hybrid technique with PBO efficiency peaking (Fig. 2) substantially enhances the PA average efficiency for high-PAPR signals. Compared with a Class-G only PA, the hybrid Class-G and DLTM operations enhance the PA PBO efficiency within each supply mode. Different from a conventional load modulation PA, the hybrid operations greatly extend the effective load modulation range by using only a 1-bit Class-G supply modulator. This achieves a superior PA efficiency in deep PBO and relaxes the required load tuning range, allowing for a simplified, compact, and low-loss load modulation network design.

In addition, the linearity of the proposed PA is ensured by the mixed-signal PA operation. By selecting proper digital control codes for the RF power DAC, Class-G supply modulator, and the load modulation network at different P_{out} levels, the AM-AM nonlinearity is minimized. At the same time, the AM-PM distortion is cancelled by dynamic analog tuning of the varactors at the digital driver outputs [6], [7].

The proof-of-concept PA is shown in Fig. 3, and it is implemented in a standard 65nm bulk CMOS process (Fig. 4). The PA load modulation network is realized by an on-chip transformer with two 3-bit switch controlled capacitors at its primary and secondary coils. The PA load modulation network is carefully designed to achieve a compact layout with complex load tuning and high passive efficiency.

The prototype PA achieves +24.6dBm peak P_{out} and 45.6% maximum drain efficiency (DE) at 2.4GHz. The measured DE values at 3/6/9/12dB PBO levels are 39.9/37/32.6/24.7%, with 1.45/1.89/2.36/2.52× improvement over the Class-B operation. By real-time Class-G and DLTM hybrid operations with mixed-signal AM and PM linearization, the PA delivers a +18.5dBm 10MSym/s 64-QAM signal with 32.6% DE and –27.8dB EVM. The total chip area is only 1.9mm^2. Compared with CMOS PAs in literatures, our design advances the state-of-the-art PA PBO efficiency enhancement with high-linearity operation and a compact silicon area.

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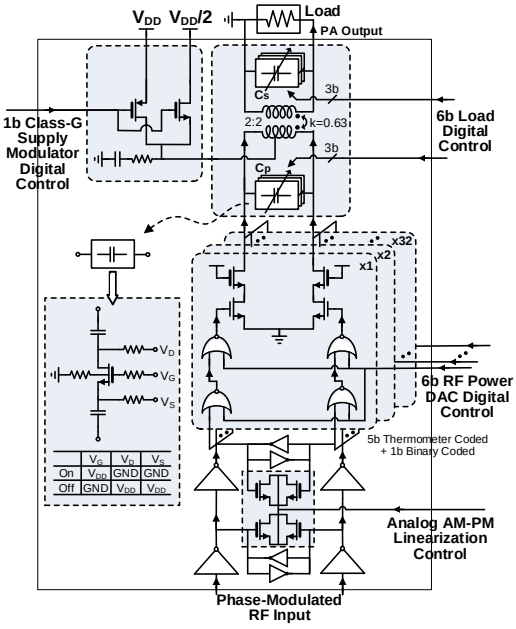

Fig. 3. Prototype PA implementation.

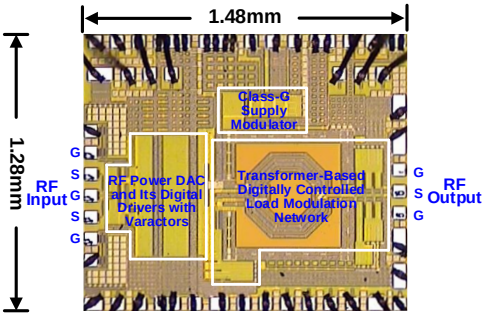

Fig. 4. Chip microphotograph.

References

[1] S. Hu, S. Kousai, J. S. Park, O. L. Chlieh, and H. Wang, "A +27.3 dBm transformer-based digital Doherty polar power amplifier fully integrated in bulk CMOS," in *Proc. IEEE RF Integrated Circuits Symp.*, 2014, pp. 235–238.

[2] S. Hu, S. Kousai, and H. Wang, "Antenna impedance variation compensation by exploiting a digital Doherty power amplifier architecture," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 580–597, Feb. 2015.

[3] S. Hu, S. Kousai, J. S. Park, O. L. Chlieh, and H. Wang, "Design of a transformer-based reconfigurable digital polar Doherty power amplifier fully integrated in bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1094–1106, May 2015.

[4] S. Kousai, K. Onizuka, S. Hu, H. Wang, and A. Hajimiri, "A new wave of CMOS power amplifier innovations: Fusing digital and analog techniques with large signal RF operations," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2014, pp. 1–8.

[5] H. Wang, S. Kousai, K. Onizuka, and S. Hu, "The wireless workhorse: Mixed-signal power amplifiers leverage digital and analog techniques to enhance large-signal RF operations," *IEEE Microw. Mag.*, vol. 16, no. 9, pp. 36–63, Oct. 2015.

[6] S. Hu, S. Kousai, and H. Wang, "A broadband CMOS digital power amplifier with hybrid Class-G Doherty efficiency enhancement," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2015, pp. 44–45.

[7] S. Hu, S. Kousai and H. Wang, "A broadband mixed-signal CMOS power amplifier with a hybrid Class-G Doherty efficiency enhancement technique," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 598–613, Mar. 2016.

[8] S. Hu, S. Kousai, and H. Wang, "A compact broadband mixed-signal power amplifier in bulk CMOS with hybrid Class-G and dynamic load trajectory manipulation operations," accepted and to appear in *Proc. IEEE RF Integrated Circuits Symp.*, 2016.