A 2.0-2.5 GHz Frequency-Selectable Oscillator for Digital Predistortion Model Identification

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***Abstract*—This paper presents the design of a variable frequency oscillator used as part of a new data acquisition architecture for the digital predistortion (DPD) of power amplifiers (PAs). The proposed architecture aims to alleviate the requirement of a high sampling rate analog-to-digital-converter (ADC) in the data acquisition loop. The oscillator utilizes switchable capacitors with a digital control scheme and is capable of operating between 2.0 and 2.5 GHz with an approximate frequency step size of 512 kHz.**

***Index terms*— Digital predistortion, model extraction, power amplifier, switchable capacitors, variable frequency oscillator**

I. Introduction

The radio frequency (RF) power amplifier (PA) is a device that converts DC power into added RF signal power in wireless transmitters. It is well known that the PA is most efficient when operating in saturation but it is highly nonlinear in this region. Digital predistortion is a digital signal processing technique that extracts the model of the PA and uses its inverse to predistort the input signal. The cascade of DPD-PA results in a linearized output signal allowing higher input power levels to be used, increasing the efficiency of the PA [1].

Before applying DPD, an accurate behavioral model must be extracted. To do so, the output of the PA is down-converted to baseband and sampled by an analog-to-digital-converter (ADC) before further digital signal processing. It is normal to characterize at least five times the input bandwidth to include the spectral regrowth introduced by the PA nonlinearities. LTE Advanced signals have 100 MHz bandwidth, and the signal bandwidth will increase further in forthcoming 5G systems, requiring ADCs to operate at multi-giga samples per second sampling rates. Current ADCs cannot cope with these high data rates, and so, alternate architectures are required which can perform the PA output data acquisition at a much lower ADC rate.

II. DPD Model Extraction

A. Time Domain Data Acquisition

Fig. 1 depicts the conventional PA data acquisition architecture. The output of the PA is down-converted from RF to baseband, and sampled by ADCs in the time domain. The parameter extraction block then compares this data with the input signal to build a model of the PA. Sampling the full output spectrum in the time domain requires very high sampling rate ADCs.

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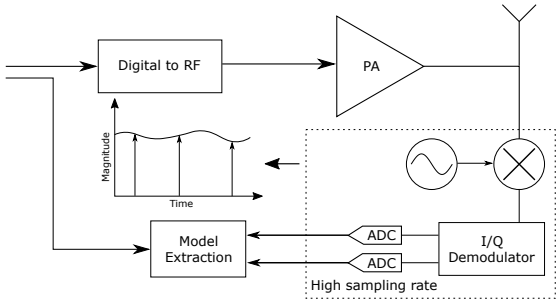

Fig. 1: Time Domain Data Acquisition

B. Frequency Domain Data Acquisition

An alternative model extraction architecture was recently proposed [2] which performs the output signal characterization in the frequency domain. It splits the output spectrum of the PA into segments and sequentially demodulates each segment, obtaining their Fourier coefficients.

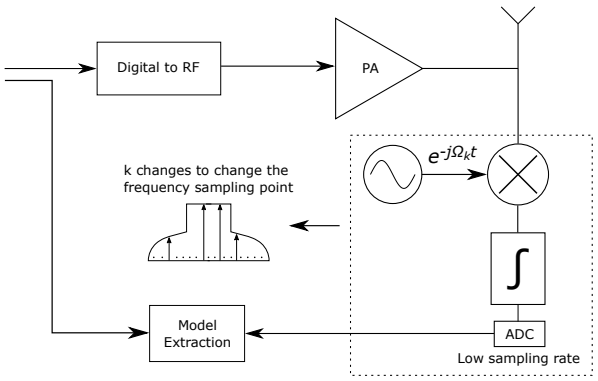

Fig. 2: Frequency Domain Data Acquisition

The architecture for the proposed solution is demonstrated in fig. 2. The output of the PA is first mixed with the complex signal $e^{-j\Omega_k t}$ where Ω_k is the characterization frequency. The output of the mixer is integrated for a period of T_0 and passed through the low rate ADC. With this operation, the sample captured at the ADC output is equivalent to the frequency domain value calculated from the Fourier transform. The local oscillator sweeps across the band, namely, by sequentially changing k, allowing the frequency domain value of the signal at different frequencies to be captured. In this approach, the ADC sampling rate is independent from the signal bandwidth which provides great advantages for future wideband applications. This paper outlines a design for the oscillator in this application.

III. Oscillator Design

The oscillator was designed using a 28nm CMOS process in Cadence Virtuoso. A complementary LC oscillator topology with tail current biasing was chosen due to its suitability to RF oscillation frequencies and its lower phase noise compared to ring oscillators. To allow for digitally controlled discrete frequency selection, a network of switchable capacitors was incorporated into the design. This network consists of two banks for coarse and fine tuning [3]. The coarse tuning bank uses a binary control coding scheme. Careful choice of capacitances results in equal frequency step sizes. The coarse bank consists of four different units resulting in 2^4 different frequency steps.

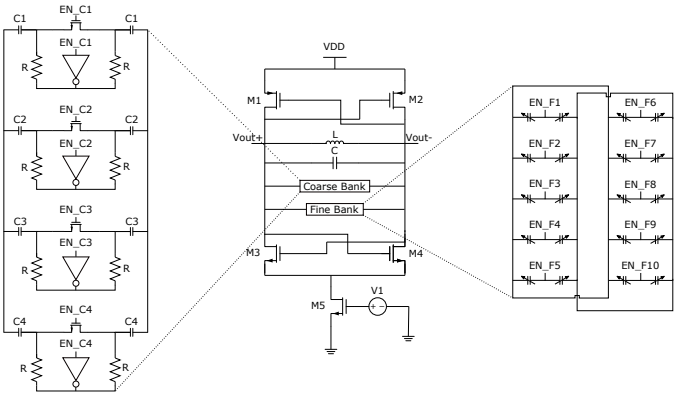

Fig. 3: Oscillator Core and Tuning Banks

The capacitance needed to change the frequency by 500 kHz was on the same scale as the parasitic capacitances of the CMOS switches used in the coarse bank. It was therefore not feasible to continue using that approach. Instead, low capacitance varactors were used with discretized control voltages. A thermometer coding scheme was used to ensure consistency of frequency step sizes. There is both an on and off capacitance associated with the units used in the coarse bank. This makes it very difficult to choose capacitance values which will result in constant frequency steps over the full tuning range. A thermometer coding scheme, linearly turning on each unit one by one, guaranteed a constant step size. 10 units were used in the fine bank.

The coarse bank, shown in fig. 3, uses resistor biasing to define a voltage between the capacitors and NMOS device while the unit is turned off. This voltage is set by the inverter and resistors R which are controlled with the same signal as the respective units. Setting the tuning range over approximately 100 MHz provided the most consistent frequency step size. Five similar designs were used in parallel, each covering 100 MHz of the full 500 MHz tuning range. The five sub ranges are controlled by connecting or disconnecting the VDD of each oscillator via an inverter. The differential outputs are connected to transmission gates which only allow the active oscillator to output a signal, minimizing interference from other circuit elements.

IV. Simulation Results

Maximum and minimum oscillation frequencies were 2.498 GHz and 2.008 GHz, respectively, resulting in a frequency

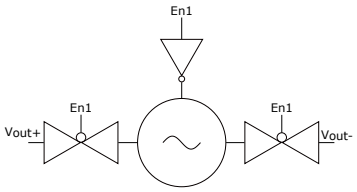

Fig. 4: One of Five Oscillator Sub-bands

range of 490 MHz and a mean frequency step size of 512 kHz. A VDD of 2.5 V was used and the active oscillator draws 1.18 mA from the supply. Phase noise was simulated at -124.5 dBc/Hz @ 1 MHz offset and -121.7 dBc/Hz @ 1 MHz offset for the minimum and maximum frequencies, respectively.

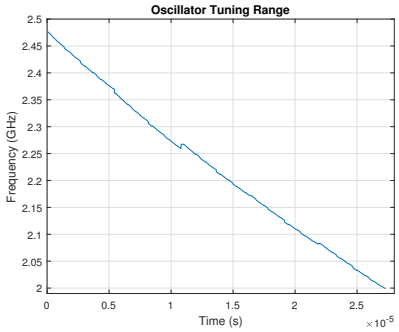

Fig. 5: Full Oscillator Tuning Range

V. Conclusion

A variable frequency oscillator was designed with a tuning range of 490 MHz and frequency step size of 512 kHz. This oscillator is a proposed solution for one circuit block as part of a new PA data acquisition architecture which aims to characterize the output spectrum of the PA in the frequency domain to alleviate the high data rate requirements for the ADC in the feedback path.

VI. Career Plans

Upon completion of my masters, I plan to get some industry experience before considering future options. This scholarship has given me a newfound appreciation of this field and has fortified my interest in a career in this area. Attending IMS opened my eyes to the global community of researchers contributing to the RF and microwave field. It was great to meet others from all over the world, to see different areas of research, and especially to see how my own project fitted into the bigger picture. It was very exciting to attend presentations from world experts which gave me the hope of someday creating something that can make a difference.

References

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