Active and Passive Device Characterizations on CMOS for Ultra-High Data-Rate Millimeter-Wave and Sub-Terahertz Wireless Transceivers

Korkut Kaan Tokgoz, *Student Member, IEEE*, and Kenichi Okada, *Senior Member, IEEE*

***Abstract*— To achieve wireless communication data-rates for more than 100 Gb/s, wideband and higher modulation complexity transceivers have to be designed and implemented. For these kinds of systems, the SNDR requirements are very challenging. Hence, the research has to be started from the accurate active and passive device designs, characterizations and modeling of these devices in order to achieve ultra-high data-rate wireless communications. Thanks to these characterization efforts, an ultra-wideband transceiver is designed accurately and implemented on 65nm CMOS achieving world's highest data-rate wireless communication of 120Gb/s from a single transceiver. The transceiver occupies 6mm^2 chip area while consuming 110mW and 177mW from 1V supply for transmitter and receiver, respectively.**

***Index Terms*— ultra-high data-rate, millimeter-wave, W-band, CMOS, frequency-interleave, de-embedding, device characterization**

I. Introduction

INTEREST in millimeter-wave (mm-wave) and sub-terahertz frequency regions keep their importance owing to several characteristics and applications. For instance; for high-speed high-data-rate wireless communication applications, bandwidth can be larger [1–4]. In the past, high-frequency research was mainly based on compound semiconductors, since the transistors in these manufacturing technologies could work on very high frequencies. Together with the continuous advancements in CMOS fabrication, the working frequencies of transistors are increased and it became possible to implement mm-wave systems in CMOS monolithically with baseband systems. CMOS technology is more complex and has more parasitics. Considering ultra-high data-rate robust, repeatable and sustainable wireless systems on CMOS, one has to start the research from device characterization and layout optimization due to several reasons. One of these reasons is that foundries generally provide PDK models of devices up to around 20GHz and these models do not provide accurate information for mm-wave and sub-terahertz frequency regions. Another reason is that custom layout optimizations for transistors and generating custom passives are required for mm-wave and sub-terahertz circuit design.

Korkut Kaan Tokgoz and Kenichi Okada are with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo, 152-8552, Japan (e-mail: korkut@ssc.pe.titech.ac.jp).

II. Description of The Project

To achieve the aim of wireless CMOS transceivers having more than 100Gb/s data-rate, the research started from active and passive device layout optimizations and characterizations [6-11]. Based on these efforts, models of custom layout active and passive devices are generated. A W-band transceiver aiming for more than 100Gb/s is designed and manufactured on 65nm CMOS [3]. This transceiver achieved 56Gb/s wireless data-rate with 16QAM and presented in IEEE ISSCC 2016 as the highest data-rate CMOS transceiver at the time [3]. One of the reason why more than 100Gb/s could not be achieved is that the models generated has some deviations at W-band. De-embedding, transmission line characterizations and pad parasitic calculation is the first and the most important step upon accurate device modeling since this is the first step for every characterization process. Transmission line characteristics in [6] have some deviations from theoretical expectations around W-band frequency region. Hence, we have improved the transmission line characteristics, pad parasitic calculations and, hence, de-embedding procedure [5]. Following to the improved de-embedding procedure, the active and passive device models became very accurate at W-band frequency regions. Improved version of [3] is implemented again on 65nm CMOS [4]. Frequency-interleaving architecture is applied and the block diagram can be observed in Fig. 1. This transceiver has a die area of 6mm^2 (Fig. 2). Measurements for the highest data-rate of 120Gb/s is shown in Fig. 3. A minimum TX-to-RX EVM of -16.9dB is achieved. This transceiver has achieved the highest data-rate of 120Gb/s from a single transceiver when compared with all of the silicon manufacturing technologies, thanks to the accurate active and passive device characterization methods.

III. Impact of MTT-S Graduate Student Fellowship, Achievements and IMS

More than anything, it is a great honor that our research is recognized by IEEE Microwave Theory and Techniques Society (MTT-S) with Graduate Student Fellowship. The first author is grateful for the support of award from the fellowship and support to attend IMS 2017 to receive the recognition certificate. It was very fruitful to attend IMS again, and have connections with professionals from all around the world with different backgrounds.

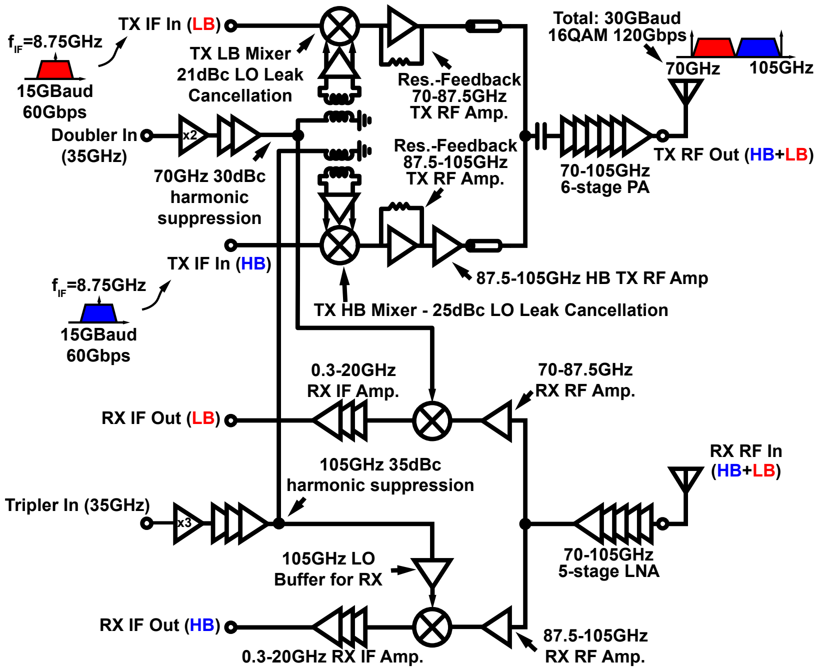


Fig. 1. W-band ultra-wideband (70-105GHz) 16QAM 120Gb/s transceiver block diagram.

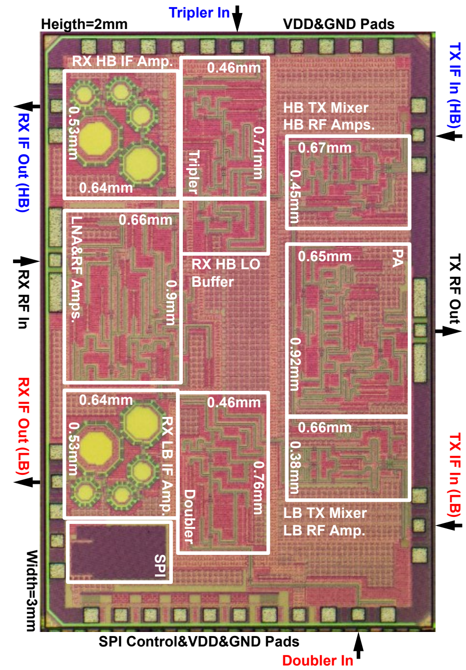
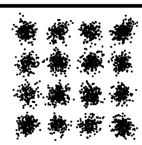
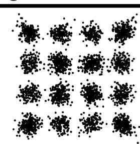


Fig. 2. W-Band transceiver chip photo.

Carrier Freq.	Low-Band 70GHz	High-Band 105GHz
TX-to-RX Constellation 16QAM*		
Symbol Rate	15GBaud	15GBaud
EVM	-16.9dB	-17.0dB
Data Rate	120Gbps	

*23dBi horn antennas are used for TX and RX. Communication distance is 0.2m including the loss from module.

Fig. 3. TX-to-RX constellation measurement results for 120Gb/s data-rate.

During the fellowship time, we have successfully achieved 120Gb/s wireless data-rate and presented in IEEE ISSCC 2018 [4]. Additionally, we have demonstrated this system in the same conference. The first author is awarded with IEEE SSCS Predoctoral achievement award 2018. With the help of the accurate device models, a low-loss 60GHz transmitter-receiver switch is successfully implemented in the same process and presented in [2]. Improved manuscript is accepted for publication in IEICE Electronic Express [1].

IV. Career Plans

Upon my graduation, I would like to experience industry for better understanding the needs of society for today and tomorrow. In the end, we are scientists and engineers mainly working for the sake of prosperity of humankind. After this short term future plan, I believe that I will be able to have better understanding of the needs which enables me to decide on my long term plans; academy, industry, etc.

References

[1] K. K. Tokgoz, S. Kawai, K. Okada, and A. Matsuzawa, “Design of Low-Loss 60GHz Integrated Antenna Switch in 65nm CMOS,” *IEICE Electronics Express* (Accepted to be published).

[2] K. K. Tokgoz, S. Kawai, K. Okada, and A. Matsuzawa, “A Low-Loss 60GHz Integrated Antenna Switch in 65nm CMOS,” *IEEE International Symposium on Radio-Frequency Integration Technology*, pp. 50-52, Seoul, Korea, Aug. 2017.

[3] K. K. Tokgoz, S. Maki, S. Kawai, N. Nagashima, J. Emmei, M. Dome, H. Kato, J. Pang, Y. Kawano, T. Suzuki, T. Iwai, Y. Seo, K. Lim, S. Sato, N. Li, K. Nakata, K. Okada and A. Matsuzawa, “A 56Gb/s W-Band CMOS Wireless Transceiver,” *IEEE International Solid-State Circuits Conference*, pp. 242-243, San Francisco, CA, Feb. 2016.

[4] K. K. Tokgoz, S. Maki, J. Pang, N. Nagashima, I. Abdo, S. Kawai, T. Fujimura, Y. Kawano, T. Suzuki, T. Iwai, K. Okada and A. Matsuzawa, “A 120Gb/s 16QAM CMOS Millimeter-Wave Wireless Transceiver,” *IEEE International Solid-State Circuits Conference*, pp. 168-169, San Francisco, CA, Feb. 2018.

[5] I. Abdo, K. K. Tokgoz, T. Fujimura, K. Okada, and A. Matsuzawa, “Comparison Between L-2L and Thru-Reflect-Line De-embedding Methods for W-Band CMOS Amplifier Design,” *IEEE International Symposium on Radio-Frequency Integration Technology*, pp. 34-36, Seoul, Korea, Aug. 2017.

[6] S. Kawai, S. Sato, S. Maki, K. K. Tokgoz, K. Okada and A. Matsuzawa, “Accurate Transistor Modeling by Three-parameter Pad Model for Millimeter-Wave CMOS Circuit Design,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 6, pp. 1736-1744, Jun. 2016.

[7] K. K. Tokgoz, K. Lim, S. Kawai, N. Fajri, K. Okada, A. Matsuzawa, "Characterization of Crossing Transmission Line Using Two-Port Measurements for Millimeter-Wave CMOS Circuit Design," *IEICE Transaction on Electronics*, vol. E98-C, no. 1, pp.35-44, Jan. 2015.

[8] K. K. Tokgoz, S. Maki, K. Okada, and A. Matsuzawa, “Characterization of Cross-Line up to 110GHz Using Two-port Measurements,” *IEEE International Symposium on Radio-Frequency Integration Technology*, pp. 97-99, Sendai, Japan, Aug. 2015.

[9] K. K. Tokgoz, K. Lim, Y. Seo, S. Kawai, K. Okada, and A. Matsuzawa, "Cross-Line Characterization for Capacitive Cross Coupling in Differential Millimeter-Wave CMOS Amplifiers," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 46-48, San Diego, CA, Jan. 2015.

[10] K. K. Tokgoz, K. Lim, K. Okada, and A. Matsuzawa, "Shunt Characterization Technique of Decoupling Transmission Line for Millimeter-Wave CMOS Amplifier Design," *IEEE Asia-Pacific Microwave Conference*, pp. 274-276, Sendai, Japan, Nov. 2014.

[11] K. K. Tokgoz, N. Fajri, Y. Seo, S. Kawai, K. Okada, and A. Matsuzawa, "A Characterization Method of On-Chip Tee-Junction for Millimeter-Wave CMOS Circuit Design," *International Conference on Solid State Devices and Materials*, pp. 94-95, Tsukuba, Ibaraki, Japan, Sep. 2014.