Self-Interference Cancelling Receiver for Single Channel Full-Duplex Wireless Communication

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***Abstract*— A single-channel full-duplex receiver is presented with tunable self-interference (SI) canceling capability. The receiver utilizes the high linearity of passive mixer-first receiver architecture and LO phase shifting to handle and cancel the SI without degrading the receiver sensitivity due to intermodulation distortion. The proposed receiver is implemented in 130nm CMOS process and shows 45 dB cancellation with 7.5 dB DSB noise figure and better than -10 dB matching at the input.**

***Index Terms*—CMOS radio receiver, mixer-first architecture, single-channel full duplex, self-interference cancellation.**

I. Introduction

Single-Channel full-duplex wireless, where a node transmits and receives on the same frequency at the same time has garnered recent research attention owing to its attractive benefits of theoretically doubling system throughput and providing additional advantages in higher networking layers [1].

The main challenge for such a radio to operate is the strong interference from its own transmitter, referred to as self-interference (SI). For typical wireless applications such as WLAN, the SI can be more than 100 dB stronger than the received signal at the same frequency. If not suppressed, the SI would saturate the receiver chain and swamp out the weak desired received signal.

The present techniques to mitigate SI can be broadly classified into two categories - *suppression* and *cancellation*. In one of the techniques in the former category, SI is prevented from coupling to the RX port by using two different antennas for TX and RX, and placing them physically apart [1]. However, owing to the compact form factor, there is a limit on antenna separation, and thus on the amount of suppression.

The latter technique is based on the fact that since the transmitted signal is known, it can be subtracted at the receiver. This technique has been the focus of current research, and it has been reported that for practical receiver designs, there must be different stages of cancellation to achieve the ultimate goal of over 110 dB overall rejection. As much cancellation as possible should be achieved early in the receiver chain to relax the specifications of the following blocks [2].

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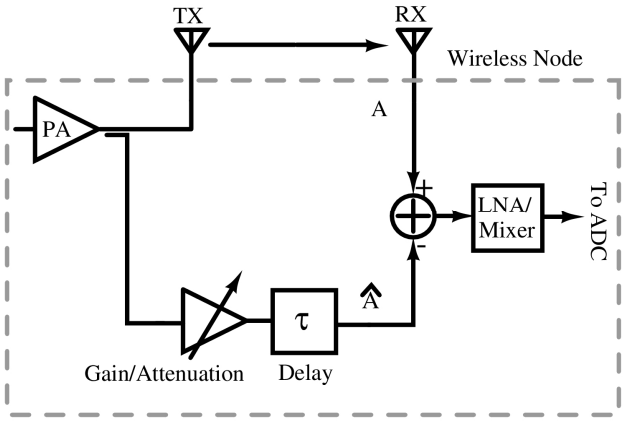

Figure 1: Block diagram of a generic self-interference cancelling receiver

II. Self-Interference Cancellation

Fig. 1 shows the generic diagram of a self-interference canceling receiver. To subtract the SI at the receiver input, a copy of the transmitted signal is tapped at the output of the power amplifier delivering power to the antenna, thus containing all TX non-idealities such as non-linearity and noise. The replica signal must be scaled in amplitude and delayed in time before subtracting at the receiver to account for the changes the SI undergoes while traveling from the TX to the RX antenna. Since generating on-chip time delay is not an area efficient solution, the time delay is often approximated as a phase shift for narrowband signals.

As the power of the SI signal is very large, the phase-shifter and RF front end must meet impractical linearity requirements so that the intermodulation distortion remains below the sensitivity level. In this work, a mixer-first receiver architecture with variable-phase LO is proposed to tackle this stringent linearity constraint.

Figure 2 shows the proposed architecture. The primary path from the RX antenna (RF_In) contains both SI and the weak desired signal. This signal is down-converted using passive mixers (Fig. 3) to give differential quadrature baseband outputs.

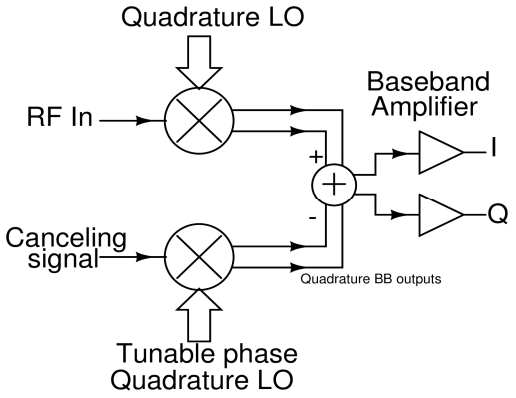

Figure 2: Proposed receiver based on mixer-first architecture.

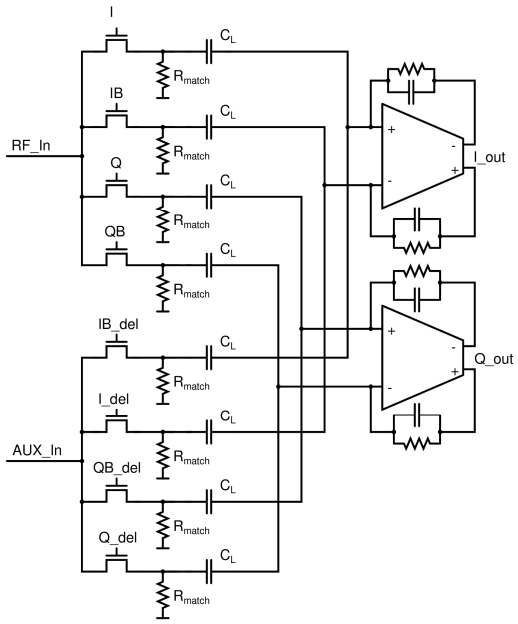

Figure 3: Circuit implementation of passive mixer and baseband summing stage.

In an auxiliary path, which is a replica of the main path, the SI alone is tapped from output of the transmitter and scaled in magnitude using an off-chip tunable attenuator. The phase of the down-converted SI in the auxiliary path is controlled by tuning the phase of the clock signal driving the corresponding passive mixer. When the amplitude and phase of the SI in the auxiliary path matches that in the main path, perfect cancellation is achieved. In practice, however, the finite resolution of amplitude and phase tuning and random mismatch between the two paths will limit the cancellation. In this work, a phase-step of 0.18 degree at 1 GHz is implemented in conjunction with the use of a continuously tunable off-chip attenuator to achieve an overall SI cancellation of 45dB. Since both paths are identical, intermodulation distortion products also get cancelled, resulting in very good linearity Performance.

Figure 3 shows the circuit implementation of the passive-mixer and baseband summer. The mixers are driven with 25% duty cycle clocks. To phase shift the LO, a combination of MUX and inverter chains loaded with digitally tunable capacitor banks is used. The input capacitor of the summing amplifier acts as the load capacitor for the passive mixer, and the currents in the main path and the auxiliary path are summed at the virtual ground node of the OTA.

RESULTS

The proposed receiver is designed in a 130nm CMOS process. The layout-extracted simulation results are tabulated in Table 1. A cancellation of better than 45 dB is achieved with LO delay tuning while handling SI level of -10 dBm at the RX input. As seen from the table, the switching power is a significant fraction of the total power, which is expected to scale down with the use of finer technology with shorter gate length.

The chip is currently in the fabrication stage and we expect to validate the idea with silicon measurements in the near future.

Noise Figure	7.5 dB
Max. tolerable SI at RX input	-10 dBm
Cancellation	45 dB
Power consumption	42 mA (switching), 32 mA baseband
Technology/ Supply	130nm CMOS/ 1.2 V
Signal bandwidth	20 MHz around LO

Table 1: Key performance parameters of the proposed receiver.

CONCLUSION

A technique to cancel the SI while achieving high linearity is implemented. The technique shows a cancellation of 45dB in post-layout simulations while handling -10 dBm SI power at the same frequency. Half of the total power is dissipated in the clock delay circuits, which is expected to scale favorably with state-of-the-art CMOS technology.

Impact of the MTT-S Pre-Graduate Award:

It has been an honor and highly motivating to receive the MTT-S pre-graduate award. The award has given me a feeling of accomplishment, and an urge to contribute back to the microwave and RF community. Attending IMS 2015 was a great learning experience on its own. I got an opportunity to meet the stalwarts of the community and discuss my work with a few of them, which gave me new ideas and insights.

As my immediate career plan, I wish to pursue a doctoral degree in the field of RFIC design.

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