A 4-bit SiGe Passive Phase Shifter for X-band Phased Arrays

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***Abstract*—This paper presents a 4-bit passive phase shifter for X-band (8-12 GHz) phased-arrays, implemented in 0.25-μm SiGe BiCMOS process. All bits are digitally controlled. The 22.5° and 45° bits are based on switched low-pass network while the 90° and 180° bits are based on switching between high-pass/low-pass filters. Filters are implemented using on-chip spiral inductors and high-Q MIM capacitors. Switching functionality is obtained by isolated NMOS transistors employing resistive body floating technique. All bits are optimized to minimize the RMS phase error. Ordering of bits is optimized so as to minimize the overall insertion loss. Overall insertion loss is 12$\pm$2 dB and RMS phase error is less than 2° over X-band frequencies.**

***Index Terms*—Low noise amplifiers, switched gain, bypass LNA, 0.25-μm BiCMOS, body-floating, X-band**

I. Introduction

MODERN phased arrays contain thousands of high-performance transmit/receive modules to achieve fast beam scanning and electronic beam control. The performance of phased arrays is mainly determined by the performance of T/R modules. Fig. 1 shows a simple block diagram of a T/R module, consisting of a low-noise amplifier (LNA), a power amplifier (PA), a single-pole double-throw (SPDT) switch, a T/R switches and finally a phase shifter (PS). The phase shifter is one of the key components of a T/R module as it determines the phase resolution of the system [1].

Due its high-performance requirements, phase shifters have been implemented with III-V technologies. However, due to the recent developments in silicon process technologies, there has been a large amount of research on Si-based highly compact and low cost phase shifters [2]. In this paper we present a 4-bit (22.5° steps) digitally controlled passive phase shifter implemented in 0.25-μm SiGe BiCMOS process.

II. Circuit Design

A passive structure has been chosen to realize the phase shifter. The 4-bit passive phase shifter is based on a hybrid topology, and can be seen in Fig. 2.

The lower bits (22.5° and 45°) are implemented using switched-filter networks. When M_5 transistor is OFF and M_6 transistor is ON, L_3 and C_4 construct a low-pass filter, which can provide up to 90° phase shift while still being matched to 50 Ω. When M_5 transistor is ON and M_6 transistor is OFF, the low-pass filter is by-passed by the very low on-resistance of M_5. Inductor L_4 resonates out the off-capacitance of M_6.

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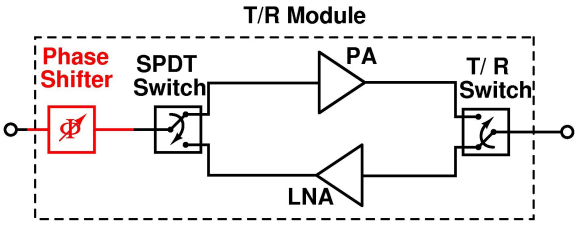

Fig. 1. Simple block diagram of a SiGe BiCMOS T/R module.

For higher bits (90° and 180°), the switched filter topology away from the center frequency, therefore, these bits are implemented by switching between high-pass and low-pass filter networks, with the cost of increased chip-area. In this topology, phase-vs.-frequency slopes of the high-pass and low-pass filters compensate each other such that a constant phase shift is obtained throughout the X-band.

$$C = \frac{\tan(\phi/2)}{Z_0\omega_0} \qquad L = \frac{Z_0 \sin(\phi)}{\omega_0} \tag{1}$$

Input/output of each bit is designed to match 50 Ω impedance. The filter networks are implemented using on-chip spiral inductors and high-Q MIM capacitors. The values of inductors and capacitors are set to achieve the required phase shift using (1). Isolated NMOS transistors are used for the switching functionality. The size of the transistors is optimized to minimize the insertion loss. The limitation is the undesired coupling to the ground via the off-capacitances of MOS transistors. To minimize this effect, the gate and also the bulk terminals are tied to control voltages and ground respectively through 10 kΩ resistors

III. Results

The 4-bit passive phase shifer is realized using IHP 0.25-μm BiCMOS process with f_T/f_{max} of 110/180 GHz. In one chip, all blocks are casceded (Fig. 3) while each bit is fabricated seperately in another version (not shown here). Inductors are custom designed in Sonnet, with Q>20. Total chip area is 0.9 mm^2. Pad-to-pad measurments are performed.

22.5°-block has 24°-30° phase shift across X-band frequencies, 2-2.5 dB insertion loss when V_{22} is low and 3.5-4 dB insertion low when V_{22} is high. 45°-block has 46°-54° phase shift across X-band frequencies with 46.3° at 10 GHz. Its insertion loss is 3-3.5 dB when V_{45} is low and 4-6 dB insertion low when V_{45} is high.

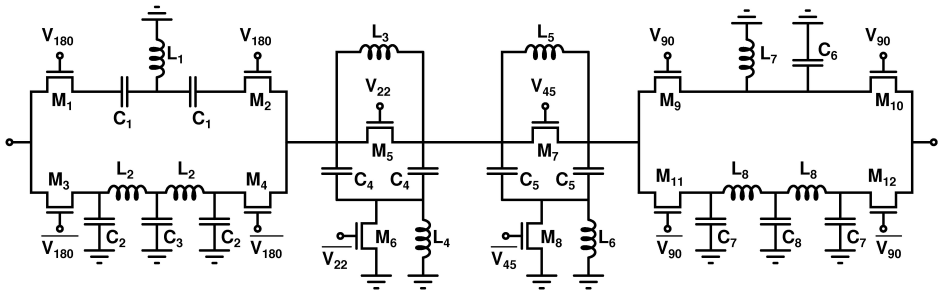

Fig. 2. Schematic of the complete 4-bit passive phase shifter.

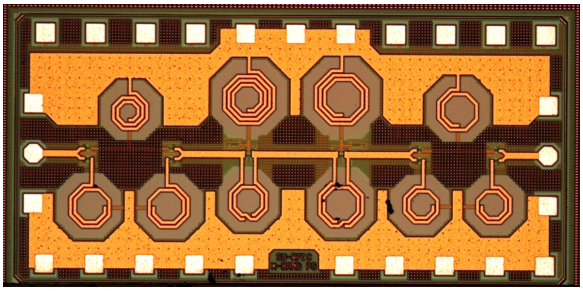

Fig. 3. Chip photo of the fabricated 4-bit SiGe X-band phase shifter.

90°-block has 87°-89° phase shift at X-band with 3.5-6 dB insertion loss. 180°-block has 178°-184° phase shift at X-band with 4-6 dB insertion loss. Input/output return losses of all blocks are better than 10 dB across X-band frequencies.

Fig. 4 shows the overall insertion phase of all 16 states, displaying linear phase shift in 9-12 GHz range while it is degraded around 8 GHz due to the 22°-block. Overall, insertion loss of the phase shifter is around 12±2 dB.

Fig. 5 shows the RMS phase and gain error of the 4-bit SiGe phase shifter. RMS gain error is below 2 dB over entire X-band and better than 1 dB in 9-12 GHz. RMS phase error is better than 8° at X-band and better than 2° in 9-12 GHz range. With these performance metrics, a SiGe phase shifter covers the requirements of X-band T/R modules to be used in phased array radars.

IV. Conclusion

A 4-bit X-band passive hybrid phase shifter in SiGe BiCMOS technology is presented. It achieves state-of-the-art RMS phase error of 2° and RMS gain error of 1 dB in 9-12 GHz range, with an insertion loss of 12 ± 2 dB. Results of this study is presented in SiRF 2013, [3].

Acknowledgment

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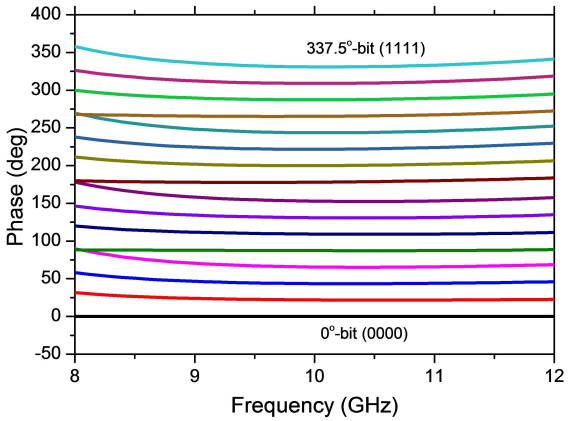

Fig. 4. Insertion phase of all 16-states.

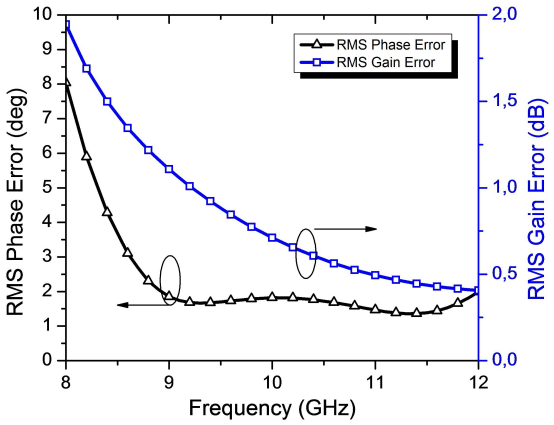

Fig. 5. RMS phase and gain error of the phase shifter.

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