Architectures and Integrated Circuits for Linearized, Watt-class, High Efficiency Millimeter-wave Transmitters in CMOS

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***Abstract*—This report addresses the research progress towards resolving the challenges associated with the implementation of efficient yet linear CMOS transmitters with watt-level output power at millimeter-wave (mmWave) frequencies. The focus has been to develop schemes for improving the back-off efficiency of high power amplifiers (PAs) through techniques such as supply modulation and adaptive biasing as well as linearizing architectures for transmitters employing such PAs.**

***Index Terms*—Power amplifier, CMOS, millimeter-wave, stacking, high efficiency, Class-E, linearizing transmitter architecture, power DAC, adaptive biasing, switched capacitor, supply modulation.**

I. Introduction

CMOS technology scaling comes at the cost of a diminution in the available supply headroom along with an increase in the loss in active and passive components. Both these features pose the bottleneck in designing high efficiency transmitters with high output power in the mmWave regime. Conventional techniques of impedance transformation and power-combining to increase output power are limited by the loss in passive components, the maximum number of elements that can be combined as well as practical layout considerations.

Typically, PAs are most efficient near P_{sat} and exhibit poor efficiency under back-off. Thus, an additional challenge arises from the trade-off between efficiency and linearity. Linearizing architectures such as Doherty and outphasing are conventionally employed to address these problems. However, the Doherty architecture requires extensive linearization while the outphasing architecture does not significantly improve back-off efficiency.

The aforementioned challenges call for innovation at both the circuit and system level. Recent work on device stacking for both linear and switching-class mmWave PAs [1], [2], [3] has successfully addressed the problem of efficient power-generation. A 3-bit power Digital-to-Analog-Converter (DAC) utilizing a novel linearizing architecture was also proposed in [3] for high efficiency under back-off and simultaneous linearization of switching PAs. However, the architecture suffers from poor peak efficiency owing to various loss mechanisms, low output power due to implementation considerations as well as low resolution. Consequently, alternative techniques are desirable which facilitate high output power, high peak as well as back-off efficiencies, linearity and high resolution.

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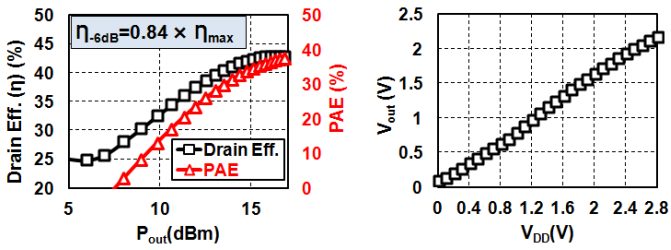

Fig. 1. Post-layout simulated (a) drain efficiency and PAE vs. output power and (b) output voltage vs. supply voltage for the 2-stacked Class-E-like PA in 45nm SOI CMOS at 45GHz reported in [2].

II. Efficient Stacked Hybrid High Power DACs

In this research, we propose the use of supply modulation in conjunction with tail transistor switching for stacked Class-E-like CMOS PAs to implement hybrid power DACs that achieve high output power as well as high peak and back-off efficiencies. The proposed technique when combined with linearization techniques can provide a complete transmitter solution.

A. Supply Modulation of Switching PAs for High Back-off Efficiency

A unique property of switching PAs is linearity in output voltage with respect to supply voltage, as shown in Fig. 1 for the 2-stacked PA reported in [2]. Ideal supply modulation also yields 84% of peak drain efficiency at 6dB back-off, which is better than Class-B PA (50%). This suggests supply modulation as a potential means of achieving high back-off efficiency. Switched-capacitor supply modulators have been adopted in this work to achieve high modulator efficiency with small form-factor, by increasing the switching frequency to a few GHz.

B. Adaptive Biasing for Stacked Switching PA Behavior

An important consideration is retention of stacked switching PA behavior (i.e equal voltage stress sharing and hard switching) under supply modulation. This can be achieved by adjusting the bias of the PA devices with varying supply voltage. We propose a novel supply-adaptive biasing scheme that ensures desired stacked PA

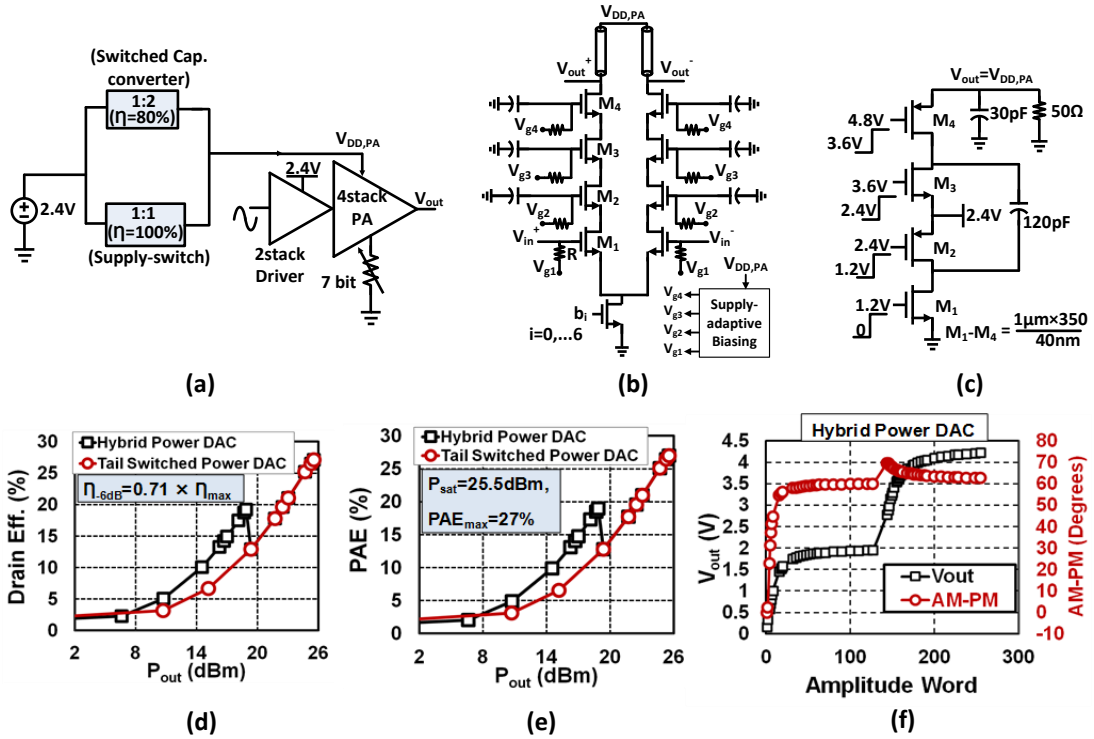

Fig. 2. (a) Proposed hybrid stacked power DAC with 4-stacked output stage using 1-bit switched-capacitor supply modulator and 7-bit tail transistor switching, (b) the 4-stacked output stage and (c) 1:2 step-up switched-capacitor converter used in the supply modulator. Pre-layout simulation results at 60GHz in 45nm SOI CMOS showing comparison of simulated (d) drain efficiency and (e) PAE of proposed hybrid power DAC with conventional tail-switched power DAC and (f) simulated output voltage and AM-PM distortion of proposed hybrid power DAC.

characteristics thereby facilitating the best possible back-off efficiency.

C. Tail Transistor Switching for High Resolution

Finally, source degeneration transistor switches as in [4] are used to incorporate high resolution into the supply modulated PAs. An important distinction from [4] is the use of the switches in the common-mode path in a differential implementation which reduces AM-PM distortion. The overall result is an efficient hybrid stacked power DAC with high peak and back-off efficiencies as well as high resolution to handle complex modulations (Fig. 2(a)-(c)). Pre-layout simulations at 60GHz (Fig. 2(d)-(f)) yield a peak output power of 25.5dBm with ≈71% of peak drain efficiency at 6dB back-off.

III. Conclusion and Future Work

The purpose of this research was to investigate and address the challenges associated with linearized, high power, high efficiency mmWave transmitters in CMOS. A stacked high power DAC utilizing switched-capacitor supply modulation and tail transistor switching with high peak and back-off efficiencies is proposed which will be incorporated in a digital polar architecture to implement a complete transmitter in 45nm SOI CMOS operating at 60GHz. Circuit techniques and transmitter architectures to further improve peak efficiency, back-off efficiency and AM-PM distortion are also being investigated.

IV. MTT-S Fellowship and Career Plan

The prestigious MTT-S Fellowship award facilitated interaction with the best researchers and enabled me to present my work on the proposed research [5] at IMS 2013. I believe the true success of innovation lies in utilizing technology to improve everyday life. Receiving the Fellowship award in recognition of my research activity was further motivation to take up challenging problems and come up with practical solutions that can be commercialized. In the immediate future, I envision a career in the industry to gain experience in the various aspects of developing a reliable end-product, while simultaneously being able to pursue research activities on exciting problems.

References

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