

Baseband signal FPGA programming for application in amplifier linearization technique that uses second harmonic

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Abstract—In this paper, the procedure of FPGA programming for the signal generation and processing for RF power amplifier linearization by the technique that uses second harmonics is presented. The proposed technique uses the modified baseband signals that modulate the fundamental carrier second harmonic. This additional signal processed for linearization is then injected at the input and output of the amplifier transistor. In-phase and quadrature-phase components of the modified baseband signal are formed as the products of the second order nonlinearity of a nonlinear system fed by the useful baseband signal. This process is realized on FPGA board.

Index Terms—linearization, amplifier, baseband signal, second harmonics, intermodulation products.

I. INTRODUCTION

According to the current trends to develop or improve the linearization techniques for power amplifiers in high speed and quality wireless communication systems, the intention of this project is to modify the linearization technique that uses second harmonics toward a baseband signal digital processing, [1]. The aim of this project is to create required in-phase and quadrature-phase baseband signals for linearization, which modulate carrier at the second harmonic. The process is performed by programming FPGA board, [2]. The modulated signal at the second harmonic is then injected at the input of the amplifier transistor together with the fundamental signal and also fed at the transistor output in order to reduce the intermodulation products. The modulated second harmonic and fundamental signal are mixed due to the second order nonlinearity of the transistor generating the additional third-order nonlinear products that may suppress the original intermodulation products distorted by the transistor nonlinear characteristic.

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II. FPGA PROGRAMMING

A system for generating the in-phase and quadrature-phase components [3] of both the useful baseband signals and the linearization signal that will be further exploited to modulate the fundamental carrier second harmonic is implemented on FPGA board. This process represents a part of the proposed technique for linearization of RF power amplifiers which block diagram outlined as Component generator is shown in Figure 1.

The main task of the Component generator, which consists of several functional units [2]-[5], is to generate and perform the modifications of the in-phase and quadrature-phase components of the baseband signal given by Equations (1) and (2), respectively, for generating the in-phase and quadrature-phase components of the linearization signals, Equations (3) and (4).

$$I = (c(t) / v_s) \cos(\varphi(t)) \quad (1)$$

$$Q = (c(t) / v_s) \sin(\varphi(t)) \quad (2)$$

$c(t)$ is the magnitude and $\varphi(t)$ is the phase of the baseband useful signal.

$$I_{lin.signal} = a_{\{i|o\}} e^{-j\theta_{\{i|o\}}} (I^2 - Q^2) \quad (3)$$

$$Q_{lin.signal} = a_{\{i|o\}} e^{-j\theta_{\{i|o\}}} 2IQ \quad (4)$$

The Component generator generates two components of baseband signal (in-phase and quadrature-phase) and four linearization components which are separately multiplied by $a_{\{i|o\}}$ for amplitude tuning and adjusted in phase by $\theta_{\{i|o\}}$ for the injection at the amplifier transistor input and output after modulation of the carrier second harmonic. Indexes i and o in subscript are related to the signals prepared for the injection at the input and output of the amplifier transistor, respectively. The baseband signal is generated in the system as the pseudo-random bits over which the procession is carried out in order to obtain the linearization components with the adequate amplitudes and phases.

Main features of systems are: working frequency is 60 MHz, generation of Linearization signal components is at frequency of 1 MHz and system supports QAM formats-16, 32, 64, 128 and 256. For the 16, 32, 64 QAM, the system meets the requirement to generate Linearization components at

a frequency of 1 MHz, while the 128 QAM generates Linearization components at a frequency of 0.85 MHz, and 256 QAM frequency components linearization signal is 1.25 MHz.

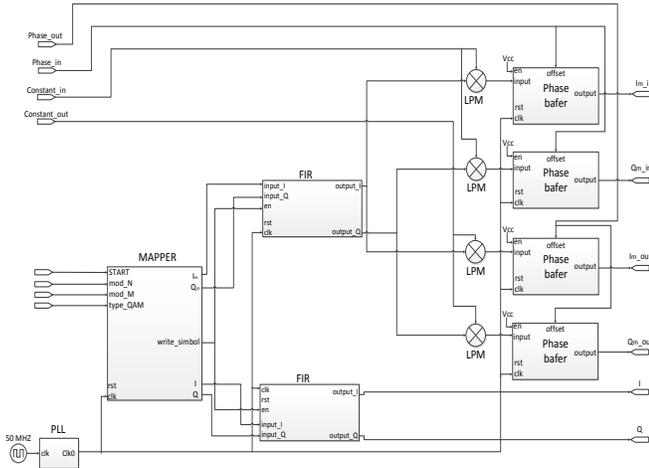


Fig. 1. Component generator block diagram

Ports of the system are divided into three groups: control signals, signals to select the type of QAM modulation and parameters of the linearization components, such as gain and phase shift, and the output ports. Table T1. shows the appropriate operations according to the value set on the ports.

T. 1. Bit rate according to the value on the port mod_N and type QAM according to the value on the port $type_QAM$

Type QAM	Port mod_N	Bit rate [MHz]	Port $Type_QAM$
16	15	4	"000"
32	12	5	"001"
64	10	6	"010"
128	8	7.5	"011"
256	7	8.57	"100"

The phase dependence of the value of the port is $\varphi = 5.7^\circ(\text{phase_in})$. The smallest phase shift is 5.7° which corresponds to the delay of the output signal from one system clock. The value on these ports "0 ... 0" relates to the zero phase shift.

The Component generator consists of two parts: the pseudo-random signal generator with QAM modulation (the left part of the block diagram - MAPPER and filters) and subsystems for the modification of the signal (the right part of the block diagram - multipliers and blocks for the phase shift). Block MAPPER provides the in-phase and quadrature-phase signal components. The filters (blocks marked with FIR) are used for narrowing the spectrum of baseband signals and linearization signals to prevent the effect of spectrum overlapping. Type of filters is rise-cosine and realized in the polyphase structure, [5]. LPM multipliers are used to multiply the received signal with a constant determined on the port, while the phase buffers are used to achieve the delay or phase shift. The outputs of the phase buffers are connected to the digital-to-analog converters which are the integral parts of the FPGA board.

System data are presented in various fixed point formats which depends on the type of modulation. Presentation of data in this format reduces the error resulting from the finite length

of the bit word and contributes to savings in hardware resources. The Figure 2 shows the signals at the output of the system.

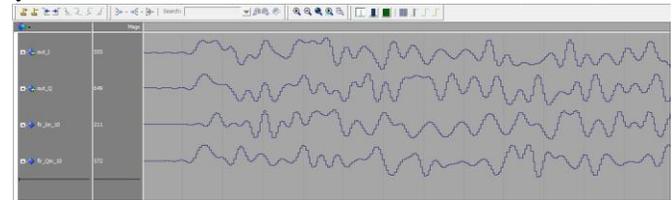


Fig. 2. In-phase and quadrature-phase components of the linearization signal which lead to input and output of the transistor

III. CONCLUSION

In this project, the baseband and linearization signals are generated and processed by FPGA board programming. The prepared signals are to be lead further to the digital-to-analog converters, the RF modulators, one related to modulation of the useful signals by using fundamental carrier and the additional modulators with the carrier at the second harmonics. Modulated fundamental signal and additional signal for linearization at the second harmonic will be then injected at the input and/or output of the transistor in amplifier circuit to suppress the intermodulation products and linearize RF power amplifier. The obtained results of linearization are intended to be sent for publication at the International Journal or Conference.

IV. CAREER

My future plans are to continue education at PhD studies in the field of microwave electronics that is my field of interest.

V. BENEFITS OF SCHOLARSHIP

Getting MTT-s scholarship has had a big influence on me in encouragement to move forward in achieving objectives and deepening of knowledge. While I was working on a project I gained a lot of new knowledge in the field of hardware implementation. Attending the conference brought me a lot of new friendships with colleagues from all around the world, a wider perspective on the development and progress of technology, experience with the latest technical resources as well as a small tourist exploring of Rome and introduction with Italian culture.

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