

# Mixed-Signal Architectures of Wideband Transmitters for High-Resolution Beamforming Transmission

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## I. INTRODUCTION

**T**HE growing demand of modern communication network with high data-rate including 5G, point-to-point backhaul systems requires energy efficiency and wideband TXs for beamforming. In the analog intensive TX architectures, DACs are essential to convert the digital baseband to analog signal. However, the power consumption of DACs with gigabits data-rate is watt-level, which decrease the system efficiency significantly especially for portable device. Meanwhile, to support high data-rate wireless transmission with high-order QAM modulations, high linearity, large dynamic range are required for TXs. Digital intensive TXs eliminate DACs, and provide solutions to break trade-off between PA efficiency and linearity [1]. A 4-element digital modulated polar phased-array TX based on phase-modulation phase-shifting is proposed [2], with state-of-the-art phase error, gain error, and system efficiency. However, the delay mismatch between the amplitude and phase path affects the modulation bandwidth, which is even more critical for millimeter-wave TX. Power-DAC based digital quadrature TX is a promising candidate for the wideband modulation at millimeter-wave bands comparing to the polar/outphasing counterparts. However, with the increasing power-DAC resolution, the parasitics of the complex interconnections of power-DAC unit cells cause efficiency degradation due to the load impedance mismatch of the unit cells. To address above issues, we propose a prototype of  $2 \times 10$ -bit digital quadrature TX [3] with notched-matching and mode-switch topology for beamforming transmission to improve the TX efficiency, bandwidth, and data-rate. To improve the scanning resolution and gain error of phased-array TX, a current-limited digital phase shifter for digital assisted phased-array TX is proposed [4]. The design mechanism with high resolution, low gain error, and wideband operation is analyzed, and a 3–7GHz prototype phase shifter is then demonstrated. Based on the mechanism [4], a 90–98GHz digital assisted phased-array TX with high phase resolution is reported [5]. The gain variation is reduced with an integrated digital assisted variable-gain PA.

In this report, we describe our recent research progress on a digital quadrature TX [3] and a digital assisted phased-array TX [5] for high resolution beamforming transmission. Fabricated in 28nm/40nm CMOS technology, the proposed

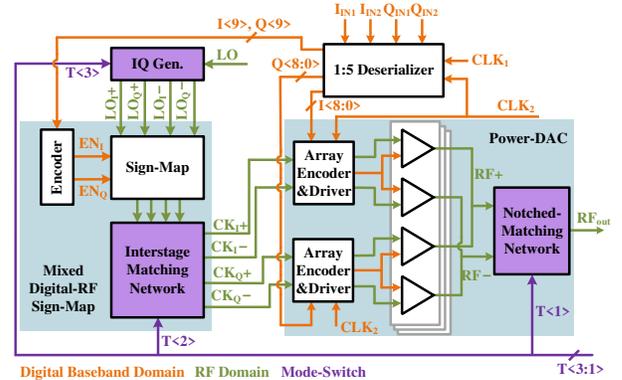


Fig. 1. Architecture of the proposed digital quadrature TX.

quadrature TX achieves the state-of-the-art power efficiency and data-rate, while the digital assisted phased-array TX achieves low RMS phase and gain errors.

## II. DESCRIPTION OF THE PROJECT

### A. 20-32GHz Digital Quadrature TX with Notched-Matching and Mode-Switch Topology for 5G Wireless and Backhaul

The proposed architecture is shown in Fig. 1. The proposed  $2 \times 10$ -bit mixed-signal quadrature TX is composed of the quadrature signal generator, mixed-signal sign-map, mm-wave quadrature power-DAC with notched-matching network, and a deserializer. The quadrature signal generator converts the input LO signal to quadrature signals. The  $2 \times 10$ -bit baseband IQ data are restored by a high data-rate deserializer from the serial inputs. The quadrant selection is realized by the mixed-signal sign-map block. The power-DAC with an array encoder, drivers, switch-cells array, and notched-matching network directly converts the digital baseband to amplified RF output. Meanwhile, the IQ generator, interstage matching of the sign-map, and output notched-matching are reconfigurable with switched capacitors to achieve a mode-switch operation, which can enhance the wideband performance of the proposed TX. A prototype of mixed-signal quadrature transmitter is fabricated in a conventional 28-nm CMOS technology, as shown in Fig. 2. It achieves the maximum output power of 19.02dBm at 22.5GHz with DE of 24.5% ( $I = 511$ ,  $Q = 511$ ), peak DE of 34.4% at 22GHz ( $I = 511$ ,  $Q = 0$ ), and peak system efficiency of 22.1% ( $I = 511$ ,  $Q = 0$ ) at 22GHz, respectively. The average DE at 6-dB PBO (22GHz) is 17.9%. 500MSym/s 64QAM and 125MSym/s 256QAM modulation signals are

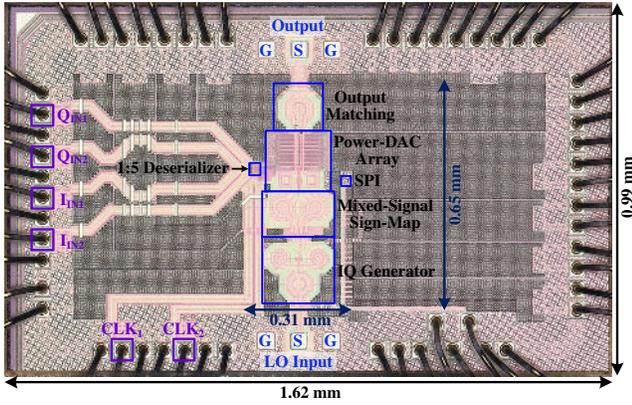


Fig. 2. Chip microphotograph of the digital quadrature TX.

measured with 4 and 16 up-sampling rate, respectively. At 23 and 28GHz, the transmitter exhibits  $\text{EVM} \leq -28.4\text{dB}$ , output power  $\geq 9.17\text{dBm}$ ,  $\text{ACPR} \leq -31.9\text{dBc}$ , respectively.

### B. A 90–98 GHz $2 \times 2$ Phased-Array Transmitter with High Resolution Phase Control and Digital Gain Compensation

A 90–98 GHz  $2 \times 2$  phased-array transmitter with 9-bit phase control and 6-bit gain compensation is proposed. The block diagram is shown in Fig. 3. The system consists of four separate transmitter channels and one 1:4 Wilkinson power divider at the input terminal. Each transmitter channel is composed of a 9-bit vector-sum phase shifter and a three-stage 6-bit digital assisted variable-gain power amplifier (DVGPA). The current source array (CSA) is introduced to implement such DVGPA. Meanwhile, the gain of DVGPA could be finely adjusted in a specific range with a small phase variation, which could minimize the gain error of the whole system. The circuits of the 9-bit vector-sum phase shifter is composed of 7-bit I-DACs, 2-bit sign control, and a I/Q generator. The L-C-R all-pass-filter is used to implement the I/Q generator. In order to decrease the imbalance of I/Q signals in the operation band, the series inductor  $L_c$  and transmission line  $T_c$  are introduced in each path to optimize the load impedance.

The  $2 \times 2$  millimeter-wave phased-array transmitter is implemented and fabricated using a conventional 40-nm CMOS technology. Fig. 4 shows the chip photograph. The whole chip size is  $2.5 \text{ mm} \times 1.1 \text{ mm}$ . Each transmitter channel is biased at 1.2 V and has a DC power consumption of 135 mW. According to the gain compensation, the RMS gain and phase errors of the proposed single channel phased-array transmitter are less than 1.12 dB and  $1.82^\circ$  at 90–98 GHz, respectively. Note that, the phase response are linearized by DPD. It can be seen that the RMS gain error is decreased in the operation band (i.e., 9.1% performance improvement at 94 GHz) with little degradation of phase error. The gain and phase variation under the 6-bit gain control states are 9.1–10.6 dB and less than  $3.65^\circ$ , respectively. The phased-array transmitter with 64 gain-control states at 94 GHz achieves 6.3–8.13 dBm saturated output power,  $>15 \text{ dB}$  gain (exclude the theoretical 6-dB loss of 1:4 power divider), and 5.9 dBm  $OP_{1\text{dB}}$  of single channel. The proposed 90–98 GHz phased-array transmitter shows merits of the low RMS phase and gain errors.

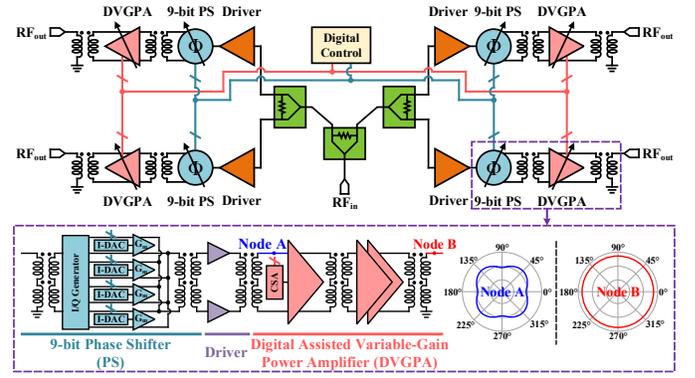


Fig. 3. Block diagram of the proposed millimeter-wave  $2 \times 2$  phased-array TX with gain compensation.

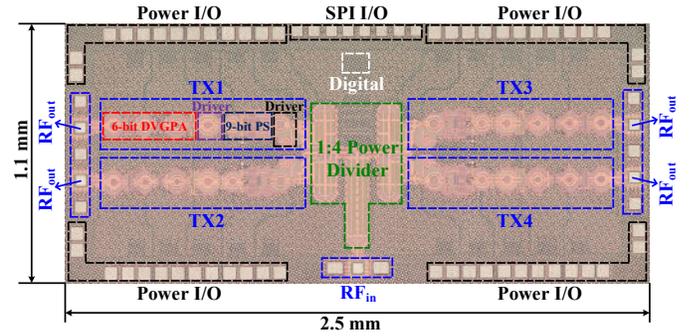


Fig. 4. Chip microphotograph of the  $2 \times 2$  digital assisted phased-array TX.

### III. FELLOWSHIP IMPACT AND CAREER PLAN

It is my great honor to receive the recognition of Microwave Theory and Technique Society for the 2018 IEEE Graduate Fellowship Award in support of my research work. This prestigious award encouraged me to continue my research in RF integrated front end. This financial support also helped me to attend International Microwave Symposium 2018, where I presented my research work, communicated with some top professionals in Microwave fields, and learn about the latest products in industry exhibition.

I plan to continue my career in academia about the wireless system, to contribute for the new generations of microwave technology and Microwave Theory and Technique Society.

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